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PHASE I OF THE AUTOMATED ARRAY ASSEMBLY TASK OF THE LOW COST SILICON SOLAR ARRAY PROJECT

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Motorola Report No. 2258/8

Final Report

January 1978

JPL CONTRACT NO. 954363

Prepared by

R. A. Pryor, L. A. Grenon, and M. G. Coleman

MOTOROLA INC. SEMICONDUCTOR GROUP
5005 East McDowell Road
Phoenix, Arizona 85005

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This work was performed for the Jet Propulsion Laboratory, California Institute of Technology, under NASA Contract NAS7-100 for the U.S. Department of Energy, (DOE) Division of Solar Energy.

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Project No. 2258

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*B: for Diagnostic Solar Cell Variables

1.0 SUMMARY

This final report brings together the two major study efforts of the second half of the contract. The first portion of the report presents the results of a study of process variables and solar cell variables. Emphasis in this portion is on identifying interactions between variables and their effects upon control ranges of the variables. The second portion of this report presents the results of a detailed cost analysis for manufacturing solar cells. This cost analysis includes a sensitivity analysis of a number of key cost factors.

The Appendix presents material which was included in the Annual Technical Report of this program, but which has required little or no change since then.

2.0 INTRODUCTION

Phase I of the Automated Array Assembly Task, LSSA Project, is concerned with a comprehensive assessment of the improvements in existing technology that may be needed to develop, within a period of no more than 10 years, an industrial capability for low cost, mass production of very durable silicon solar photovoltaic modules (and arrays).

This portion of the Phase I study involves the definition and analysis of control parameters of individual process steps as well as the integrated process sequence, and of the effects of these control parameters on the final solar cell (and module) structure, performance, and cost effectiveness.

3.0 ANALYSIS OF VARIABLES

3.1 DEFINITION OF SOLAR CELL AND SOLAR CELL VARIABLES

Studies of control variables for solar cell manufacturing must start with a definition of the desired solar cell structure, which can be related to the properties of the cell, and, in turn, related to desired process results for given process steps and sequences. Ultimately, it is desired to relate solar cell variables (and their variations) to process variables (and their control limits).

The solar cell which is considered for these studies is a silicon solar cell with a shallow ($<1\mu$) metallurgical P-N junction, a back surface high-low junction (enhancement layer), and patterned front and full back contact metallizations. The cell also has an antireflection coating covering a texture-etched front surface.

The solar cell may be characterized by a variety of operational and diagnostic variables, which can be classed as electrical, physical, or mechanical, and primary or secondary. Ultimate observation of the cell will be based upon the operational variables, while control of these operational variables will rely heavily upon control of the diagnostic variables.

Operational variables are those properties of the solar cell which are observed when the cell is either being interconnected and encapsulated or when the cell is functioning in test or service.

Cell variables which affect the operational variables are classed as diagnostic variables. Changes in operational variable values for a solar cell should be capable of correlation with changes in one or more of the diagnostic variables.

Table 1 lists the primary operational variables and Table 2 lists the primary diagnostic variables for solar cells.

In addition to the quantitatively defined variables shown in Tables 1 and 2, an additional primary cell variable is the degree of front surface (and/or back surface) deviation from flatness due either to surface texturing or to warpage. Attempts will be made to quantify this factor.

Two other primary variables are of major importance to the LSSA Project, but are considered beyond the scope of this study. First, potential interfacial interactions within the module (such as surface chemical reactions, interfacial migration, electrochemical processes, and thermal stressing) are too complex to analyze adequately in the period of time devoted to this study. Second, reliability of a solar cell in its environment as part of a module is a subject which would require long term testing of appreciable numbers of modules. In both cases, wide variations in module design and construction by the solar module industry make current studies of entire configurations premature.

TABLE 1

PRIMARY SOLAR CELL OPERATIONAL VARIABLES

Short Circuit Current, I_{sc} (T)

Open Circuit Voltage, V_{oc} (T)

Maximum Power, P_{max} (T)

Cell Conversion Efficiency, η (T)

Voltage at Maximum Power, $V_{P_{max}}$ (T)

Current at Maximum Power, $I_{P_{max}}$ (T)

Fill Factor, FF (T) = $P_{max}/(I_{sc})(V_{oc})$

Cell Series Resistance, R_{series}

Cell Shunt Resistance, R_{shunt}

Cell Thickness, t

Cell Diameter, D

Cell Length, L

Cell Width, W

Cell Area, A

Cell P-N Junction Area, A_J

Metallization Area, A_M

Metallization Coverage, A_M/A_J X 100%

Metallization Pattern Dimensions, t_M, W_M, L_M

Contact Placement

TABLE 2

PRIMARY SOLAR CELL DIAGNOSTIC VARIABLES

P-N Junction Depth, x_j

Metallization Penetration Depth, x_m

P-N Junction Layer Sheet Resistivity, ρ_{sj}

Metal Sheet Resistivity, ρ_{sm} (for each metallization width)

Back Surface (enhancement layer) Sheet Resistivity, $\rho_{s\ back}$

Back Surface High-Low Junction Depth, $X_{j\ back}$

Substrate Bulk Resistivity, ρ

Front Surface Dopant Concentration, C_S

Back Surface Dopant Concentration, $C_{S\ back}$

Dopant Profiles, $C(x)$; $C_{back}(x)$.

Crystal Orientation, (hkl)

Dislocation Density $N_{\perp}$

Spectral Response of Short Circuit Current, $I_{SC}(\lambda)$

Minority Carrier Lifetime, τ

Diode Dark Characteristics, I vs V

Surface Recombination Velocity, S

Front Surface Reflectivity, $R(\lambda)$

Base Thickness, W_B

Metal Adherence, M

Uniformity (of Operational and Diagnostic Variables over the Surface of the solar cell.)

3.2 DISCUSSION OF MAXIMUM SOLAR CELL SIZE

The lateral dimensions of silicon sheets to be fabricated into solar cells and encapsulated into modules are of major importance with respect to sheet (or crystal) growth, solar cell efficiency, manufacturing costs, and interconnection and encapsulation costs.

The current and power generated from a solar cell are area dependent. Accordingly, to a first approximation, it may be assumed that the same power can be generated from several large cells having the same total silicon area as many small cells. Upon closer examination, however, it can be seen that trade-offs exist as the cell size increases, placing a limit on the size of a solar cell from the standpoints of both cell output efficiency and cost effectiveness.

The primary argument for increasing solar cell size is to achieve economies resulting from minimizing the number of units being handled through a processing sequence and the number of cells to be interconnected prior to encapsulation. This argument assumes that the equipment utilized can process units at approximately the same rate, regardless of size, and that equipment for handling different sizes of sheets costs nearly the same amount. A great deal of support for this argument can be made by analogy to the overall semiconductor industry. There, wafer size has increased from early diameters of 0.7 inch through 2 and 3 inches and up to 5 and 6 inches in the course of less than fifteen years. This dramatic size increase is justified primarily on the basis of handling economy. There are many recorded cases of severe yield reduction when larger wafers were introduced into various semiconductor device and integrated circuit product lines. Specific process R&D effort has gone a long way towards improving yields with larger silicon wafers. However, even though the yield in terms of good units per unit area of silicon may be lower for larger wafers than for smaller ones, the increased throughput

and reduction of edge loss combine to make the use of larger wafers economically favorable.

For solar cells, however, other factors limit the maximum favorable size of the device. As cell size increases, processing equipment must become more sophisticated (and expensive) in order to achieve control and uniformity over the larger area, ultimately offsetting economies of handling. If any yield-loss mechanisms which are fundamentally area dependent exist, larger cells would mean higher costs due to increased yield loss. Conceptually, at least, future technology advances could minimize the effects of these limitations.

The most important limiting factor on large solar cell dimensions is a fundamental design consideration: increased cell size ultimately requires increased percentage metallization coverage in order to maintain a constant voltage drop per unit area in an effort to maximize cell output power. Increased metal coverage, however, results in shadowing of active cell area and reducing available power generating area. Hence, active area must be traded against increased series resistance, in order to achieve an optimal design to minimize efficiency loss as cell size increases.

While these (and similar) arguments have been widely discussed, few attempts have been made to put the limitations on cell size on a quantitative basis. An approach is presented in the following discussion to quantify these design trade-offs and to evaluate the cost effectiveness of increased solar cell sizes.

3.2.1 EFFICIENCY CONSIDERATIONS

In order to study quantitative effects of solar cell dimensions on performance and cost effectiveness, it is necessary to establish a reference model for a solar cell on which calculations and discussion can be based. Such

a reference cell has been formulated, having parameters which are of high quality. It is recognized that volume production may result in solar cells of lower quality than the model. The high quality cell has been chosen, however, to identify optimum conditions for determining cell dimensions and cost effectiveness, recognizing that in practice a cell of this quality must have smaller dimensions than calculated here. Restated, this approach identifies maximum desirable dimensions, with actual dimensions perhaps being smaller.

This approach, in turn, will place an upper limit on the size goals that the sheet and crystal growers may utilize in defining their processes.

The reference solar cell is chosen to be an ideal silicon diode with electrical contacts at the perimeter. When exposed to a solar insolation (air mass one) of $100 mW/cm^2$, the reference cell is assumed to have a generation current density, J_{gen}, of $40.0 mA/cm^2$ and an open circuit voltage, V_{oc}, of 0.600 volt. These properties relate to the silicon substrate, p-n junction, and silicon surface condition. The effect of metal covering (and thus shadowing) the front surface must still be included. Using the ideal diode equation, the generation current density and open circuit voltage may be used to calculate the diode saturation current density, J_{sat}. Thus,

$$J_{out} \cong J_{gen} - J_{sat} \exp[qV/kT]; \qquad (1)$$

$$0 = J_{gen} - J_{sat} \exp[qV_{oc}/kT]; \qquad (2)$$

$$J_{sat} = \frac{J_{gen}}{[\exp qV_{oc}/kT]} . \qquad (3)$$

From equation (3), the reference cell has a saturation current density of $3.48 \times 10^{-9} mA/cm^2$.

As stated earlier, power output and conversion efficiency will depend directly on solar cell size. Larger cell sizes generate greater currents and

require longer metal paths from the cell center to the perimeter. Longer current conduction paths require increased front surface metal coverage, or increased metal thickness, if series resistance is not to be increased. Increases in series resistance result directly in reduced cell efficiency. Therefore, the relation between cell surface area, series resistance, and power conversion efficiency must be evaluated. This is done by utilizing the ideal diode equation.

Let A be the total solar cell front surface area (in cm^2, including metal coverage), and let R be the series resistance (in ohms). The equation describing the electrical behavior becomes

$$AJ_{out} \cong fAJ_{gen} - AJ_{sat} \exp\left(\frac{q}{KT}[V+RAJ_{out}]\right) \qquad (4)$$

J_{out} and J_{sat} are calculated on the basis of total values and total surface area of the solar cell, so that

$$J_{out} = I_{out}/A \qquad (5)$$

and

$$J_{sat} = I_{sat}/A \qquad (6)$$

J_{gen} is the photogenerated current per unit area of exposed surface, and f is the fraction of the cell surface that is not covered with metal (i.e., the fraction of cell surface is exposed).

Solving the above equations for voltage, V, yields

$$V = \frac{kT}{q} \ln\left[\frac{fJ_{gen} - J_{out}}{J_{sat}}\right] - RA\,J_{out} \qquad (7)$$

Power, P, is voltage times output current.

$$P = VAJ_{out} \qquad (8)$$

$$P = \frac{kT}{q} A\,J_{out} \ln\left[\frac{fJ_{gen} - J_{out}}{J_{sat}}\right] - RA^2J^2_{out} \qquad (9)$$

Differentiating,

$$\frac{dP}{dJ_{out}} = A\frac{kT}{q} \ln\left[\frac{fJ_{gen} - J_{out}}{J_{sat}}\right]$$ (equation continued)

$$- A \frac{kT}{q} J_{out} \left[\frac{1}{J_{sat}}\right] \cdot \left[\frac{J_{sat}}{fJ_{gen} - J_{out}}\right] - 2\, RA^2\, J_{out} \tag{10}$$

By definition, at maximum output power the voltage $V = V_m$ and the current density $J_{out} = J_m$. To solve for J_m, set $dP/d\,J_{out} = 0$.

The resulting non-linear equation is

$$RA = \frac{1}{2} \frac{kT}{q} \frac{1}{J_m} \left\{ \ln \left[\frac{fJ_{gen} - J_m}{J_{sat}}\right] - \frac{J_m}{fJ_{gen} - J_m} \right\} \tag{11}$$

where RA is expressed in KΩ cm^2 when the current densities, J, are in mA/cm^2. From equations (7) and (11),

$$V_m = \frac{kT}{q} \ln \left[\frac{fJ_{gen} - J_m}{J_{sat}}\right] - RA\, J_m \tag{12}$$

$$V_m = \frac{1}{2} \frac{kT}{q} \left\{ \ln \left[\frac{fJ_{gen} - J_m}{J_{sat}}\right] + \frac{J_m}{fJ_{gen} - J_m} \right\}. \tag{13}$$

A graphical solution to these equations can be obtained by determining values of RA and of V_m for various J_m values. By forming the product of V_m and J_m, the maximum power density P_{dm} (in mW/cm^2) is obtained. Since the solar input power density is assumed to be 100mW/cm^2, the P_{dm} value is numerically equivalent to percentage cell efficiency, η. Values of P_{dm} (and/or η) are plotted against RA in Figure 1 as a function of [100(1-f)], the percentage of the total front surface area covered by metal. Values used for J_{gen} and J_{sat} are those assumed for the reference cell discussed earlier. It can be observed that as the RA product increases, cell efficiency falls off rapidly, asymptotically approaching zero independent of metal coverage. As the RA product is reduced, cell efficiency saturates at a level dependent upon shadowing by the front surface metal. Note that at a reasonable value of 5%

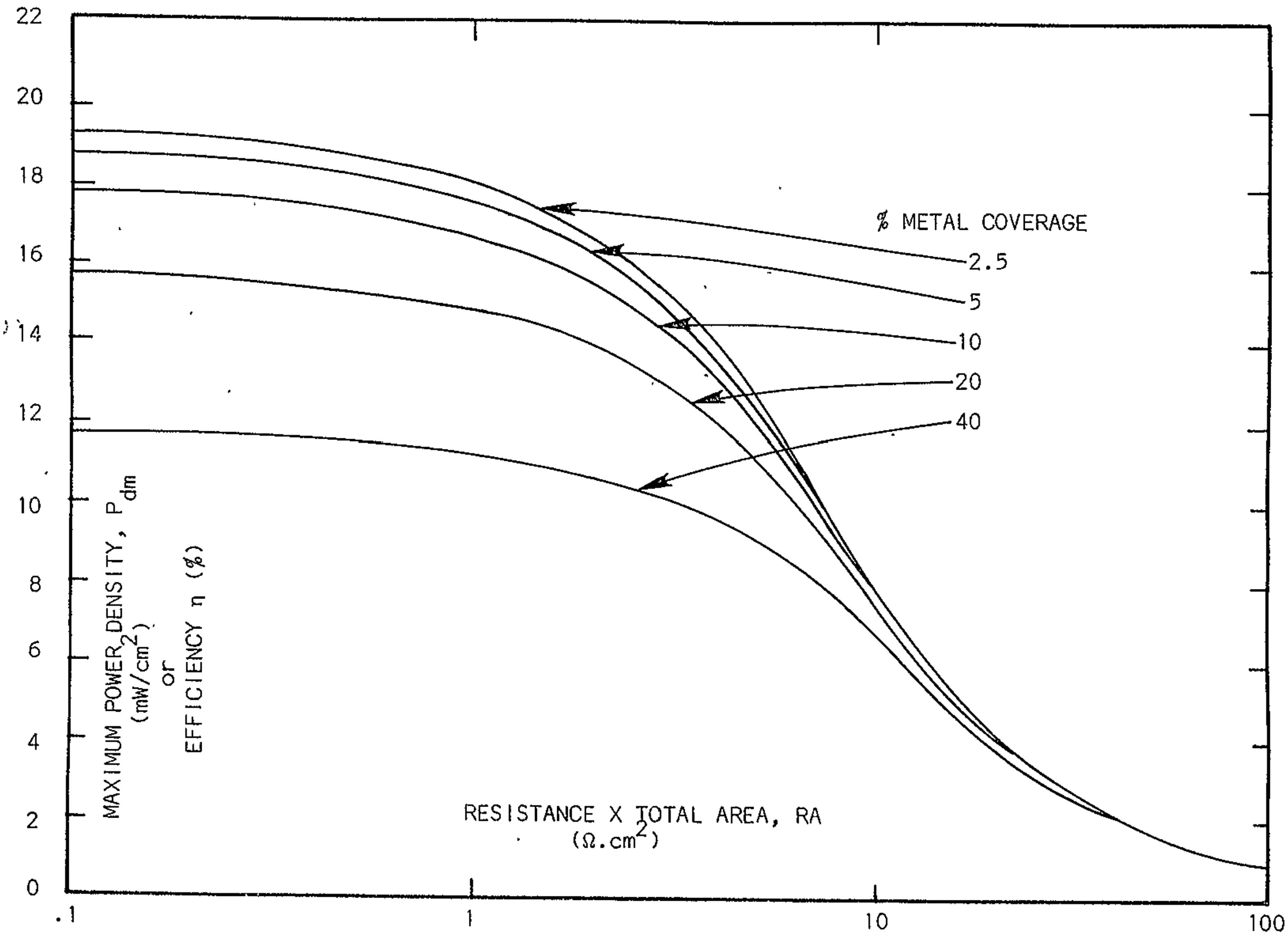

FIGURE 1: EFFICIENCY OF IDEAL REFERENCE SOLAR CELL VERSUS RESISTANCE-AREA PRODUCT, SHOWN AS A FUNCTION OF FRONT SURFACE METAL SHADOWING.

metal coverage, the parameters assumed for the reference cell allow a maximum cell efficiency of 18.6%. The reference cell has been assumed to be a very good quality solar cell.

Discussion up to this point has been general, not specifying the actual geometry of the cell or its metallization pattern. To understand the manner in which cell size influences cell efficiency, a specific example will be considered. Both cell shape and metal pattern design must be specified, as well as the diffused layer sheet resistance. To keep things as fundamental as possible, the cell is assumed to be fabricated on an infinitely long rectangular ribbon (to avoid accounting for end effects) which can be increased in width from a minimum of 2cm to any desired value. (This infinitely long cell assumption is a convenience for calculations, and does not materially effect the resulting conclusions). The metal pattern is assumed to be a grid of parallel lines running across the width of the ribbon and wrapping around both sides to eliminate the need for additional metal busses on the top cell surface. As a result, external electrical contacts to both sides of the ribbon are made on the bottom surface where the grid lines wrap around. As long as such electrical contacts are constrained to be at the perimeter of the cell (rather than through holes or channels within the center of the cell area) this metal pattern should be representative of a near-optimum design. It should be noted at this time that external wraparound contacts at all edges would allow a lower series resistance for the front surface pattern than allowing these contacts only at two edges, accommodating a somewhat larger solar cell size with the same performance as a smaller cell with contacts at two edges. This effect is maximum for a square geometry; the effect decreases as the rectangular shape increasingly deviates from that of a square. For shapes with an aspect ratio of three or four with respect to edge lengths, the two-edge contact assumption is reasonably accurate for present discussions. (Round cells have sufficiently poor

module packing factors that they are not considered here.)

The analysis is simplified by considering a 2cm long slice from the center of the ribbon as shown in Figure 2. The infinitely long ribbon can be considered to be an infinite number of these two-centimeter-long segments connected in parallel. In the data to be presented, the width of the segment was varied from 2cm to greater than 250cm. Therefore, the starting reference point is a 2cm x 2cm cell. The p-n junction is assumed to have been formed such that the front surface layer sheet resistance is 40 ohms per square. The metal pattern is assumed to have eight grid lines in the 2cm segment and the metal itself is assumed to have a sheet resistance of 0.01 ohms per square, a reasonable value for low cost metals. (Other calculations are presented in which the number of grid lines and the resistivity of the metal are varied.)

The task is now to determine cell efficiency (output power density) versus cell size (in this example, versus the ribbon cell width) for various percentages of metal coverage, for different metal thicknesses, and for different densities of metal lines. This can be accomplished by computing the solar cell resistance as a function of the parameters above, forming the product of resistance and cell area and then using the curves of Figure 1 to determine efficiency or output power density.

For this purpose, solar cell resistance is calculated in a fashion identical to base spreading resistance calculations for transistors: resistance is equated to average voltage loss divided by total output current. Lateral conduction of current through the diffused surface region and conduction of current through the metal paths each contribute a component to the voltage loss. It is assumed that the resistance to current flow vertically through the silicon substrate is negligible. The total solar cell is divided into units as shown in Figure 3, each unit having a single metal stripe. Accounting for the distributed effect of current generation and collection, the resistance of a

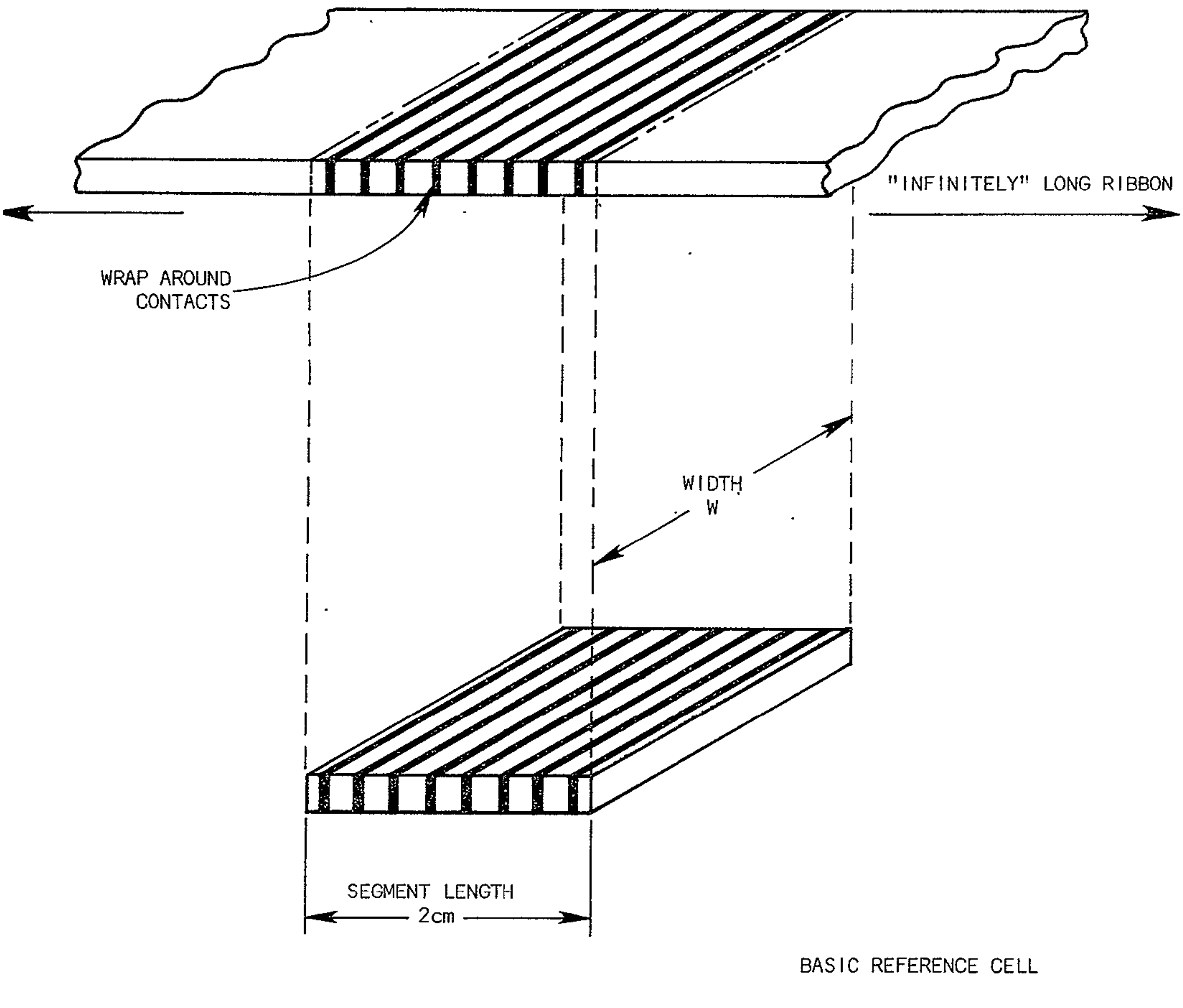

FIGURE 2: SCHEMATIC OF BASIC REFERENCE CELL SEGMENT CONSIDERED FOR COST-EFFECTIVE CELL SIZE TRADEOFFS.

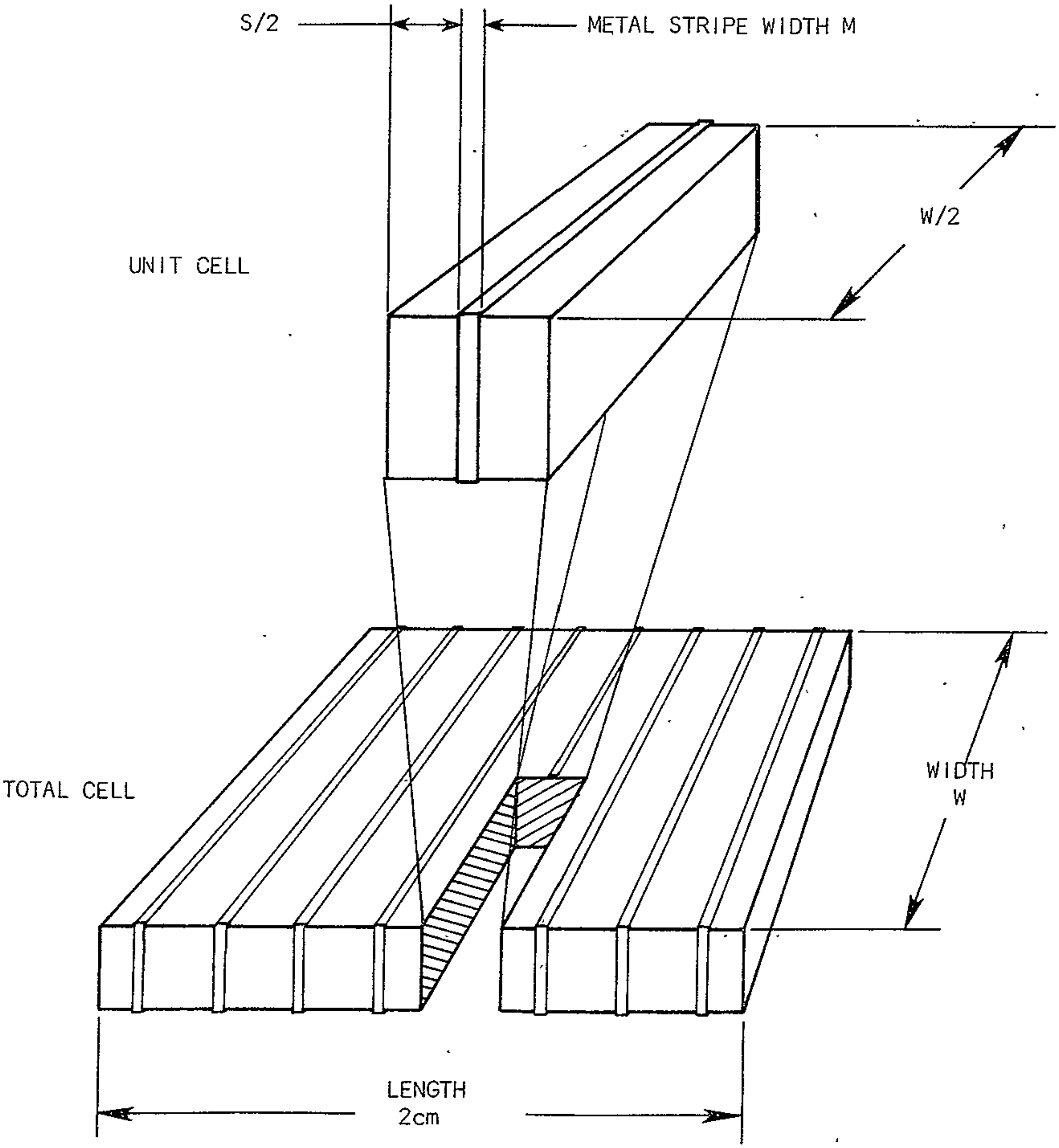

FIGURE 3: DIAGRAM OF "UNIT CELL" SECTION OF BASIC REFERENCE CELL, USED FOR SERIES RESISTANCE COMPUTATIONS.

single unit is

$$R_u = \frac{1}{3} \rho_m \frac{W/2}{M} + \frac{1}{12} \rho_s \frac{S}{W/2} \qquad (14)$$

$$R_u = \frac{1}{6} \rho_m \frac{W}{M} + \frac{1}{6} \rho_s \frac{S}{W} , \qquad (15)$$

where ρ_m is the sheet resistance of the metal and ρ_s is the surface sheet resistance of the silicon. If the number of the metal stripes in the 2cm length of the cell is N, then there are 2N unit cells in parallel and the total resistance is

$$R = \frac{R_u}{2N} \qquad (16)$$

$$R = \frac{1}{12N} \left[\rho_m \frac{W}{M} + \rho_s \frac{S}{W} \right] \qquad (17)$$

Forming the RA product yields

$$RA = [R] \; [2W] \qquad (18)$$

$$RA = \frac{W}{6N} \left[\rho_m \frac{W}{M} + \rho_s \frac{S}{W} \right] \qquad (19)$$

Equation (19) can now be used with the graphical solutions shown in Figure 1 to illustrate cell efficiency as a function of solar cell width for the particular model chosen and for variations of various front surface metal configurations. These new graphical solutions are shown in Figures 4, 5, and 6. Figure 4 shows the effect of varying metal line width such that front surface shadowing varies from 2.5% to 40% (using 8 lines per 2cm segment for all five cases shown.) Figure 5 shows the results of holding surface metal coverage at a constant 10% but varying the number of lines per 2cm segment from 4 to 8 to 16. Figure 6 exhibits the effect of doubling the metal line thickness (not width) such that sheet resistance is halved. In all cases, the curve shapes are identical, being saturated at a level of efficiency determined by metal shadowing until the ribbon width is increased by a factor of five or ten, then falling rapidly

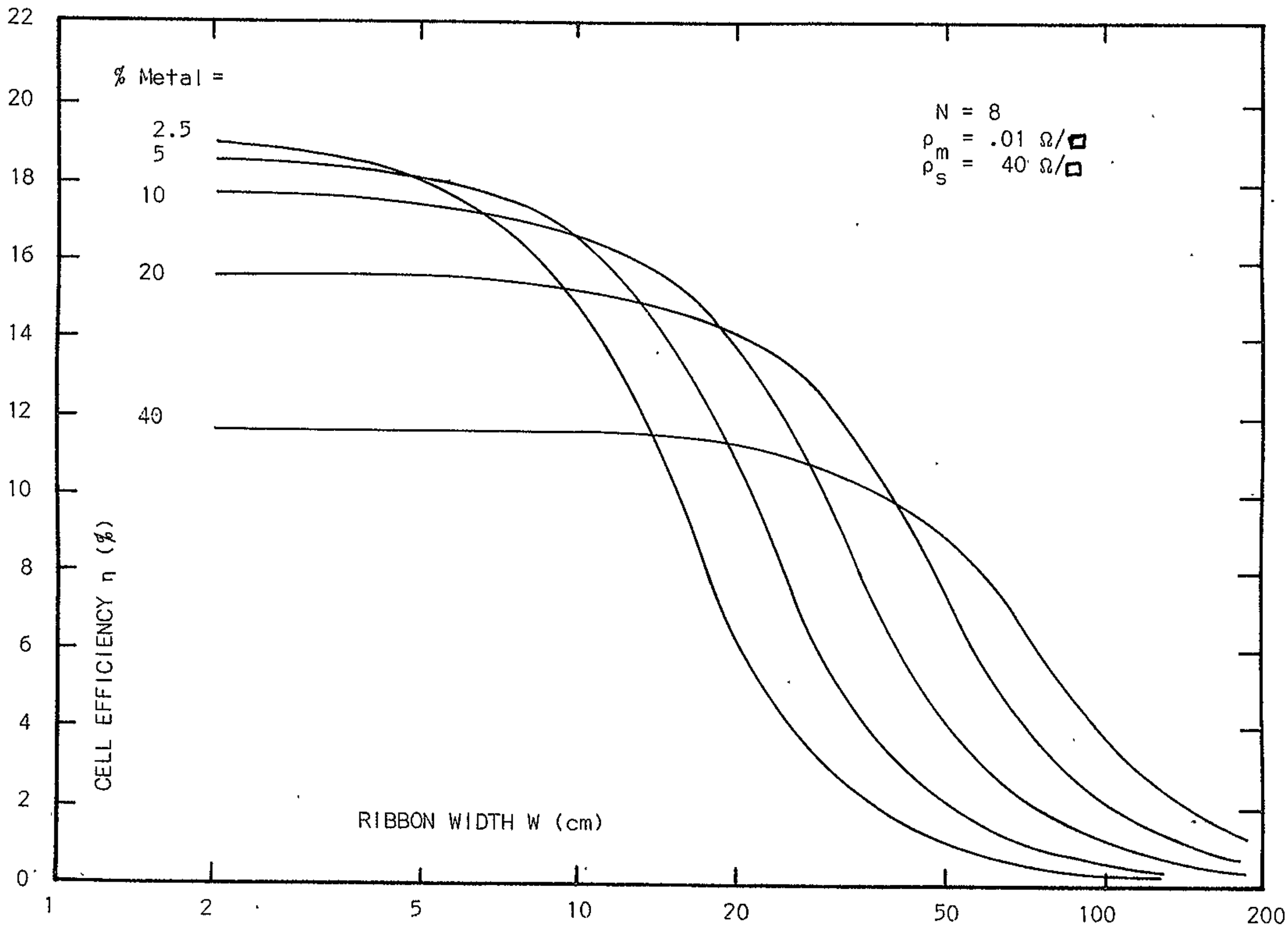

FIGURE 4: SOLAR CELL EFFICIENCY VERSUS RIBBON SUBSTRATE WIDTH, AS A FUNCTION OF METAL LINE WIDTH (i.e., FRONT SURFACE SHADOWING)

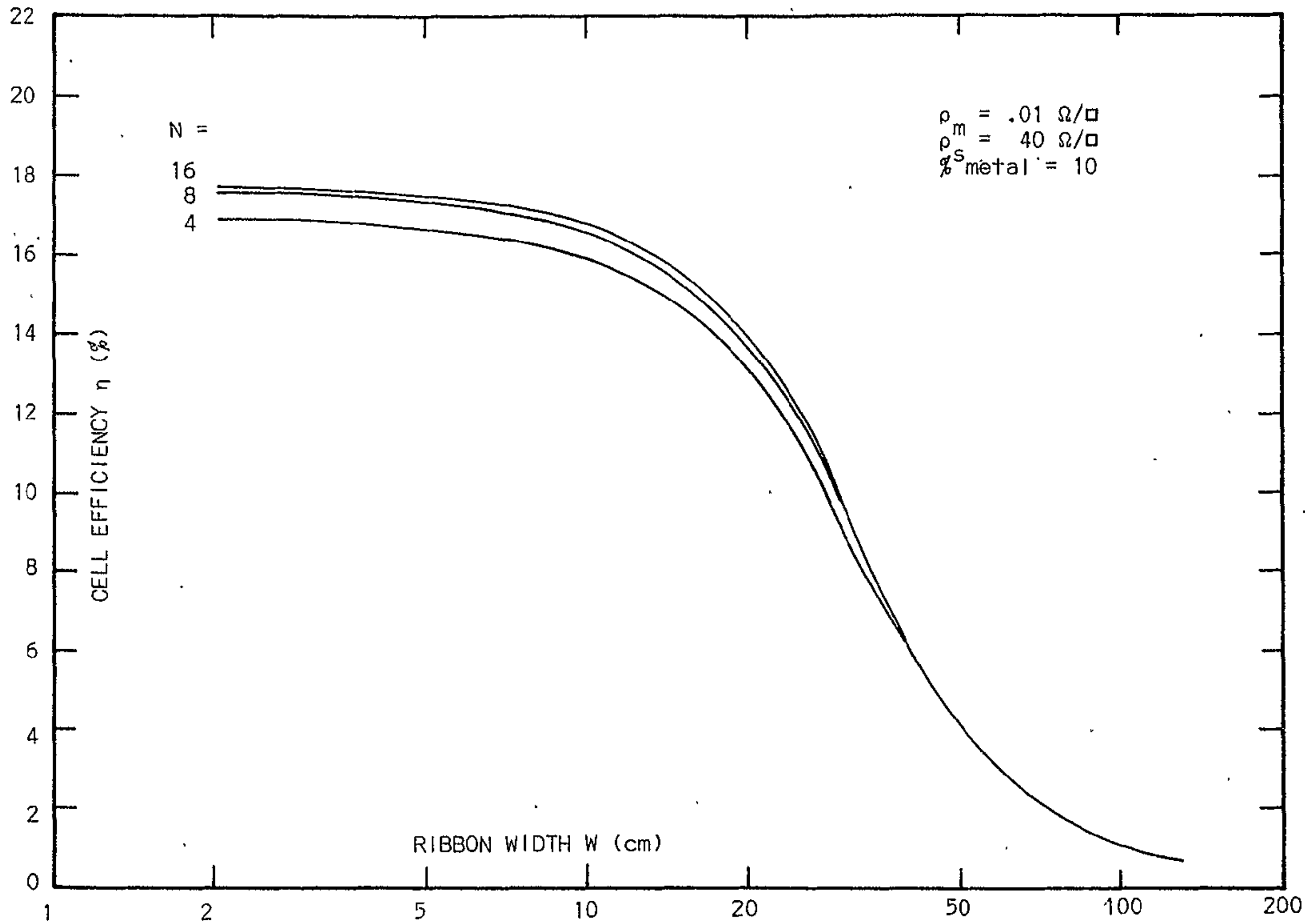

FIGURE 5: SOLAR CELL EFFICIENCY VERSUS RIBBON SUBSTRATE WIDTH, AS A FUNCTION OF NUMBER OF METAL STRIPES.

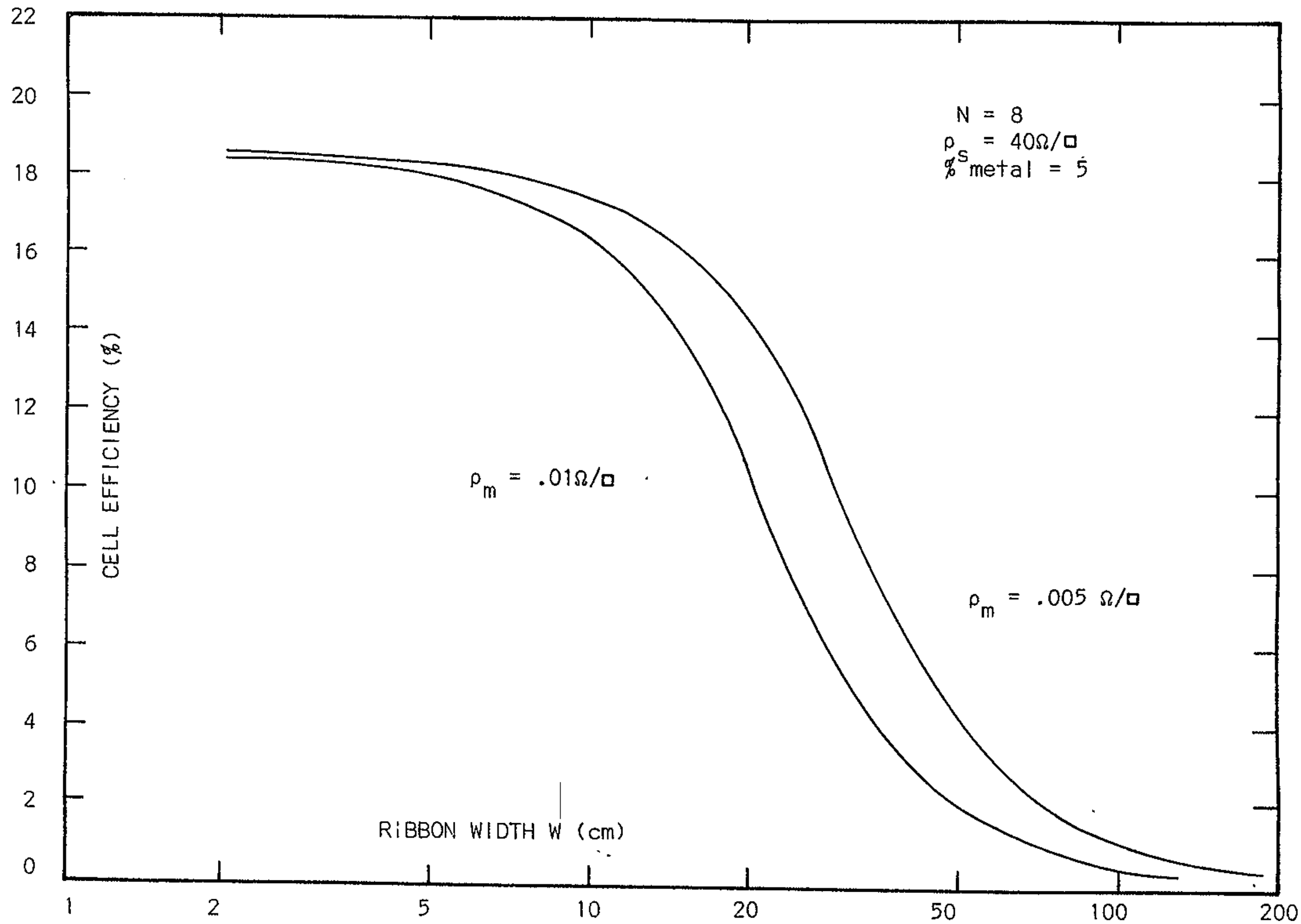

FIGURE 6: SOLAR CELL EFFICIENCY VERSUS RIBBON SUBSTRATE WIDTH, AS A FUNCTION OF METAL SHEET RESISTANCE (i.e., METAL LAYER THICKNESS)

and asympotitically approaching zero efficiency for ribbon widths greater than one hundred times the original 2cm.

The curves presented for the examples of Figures 4, 5, and 6 may be used, then, to determine a maximum allowable ribbon width if solar cell efficiency is not to drop below some arbitrary level such as 15% or 10%. As a general summary, these data indicate that ribbon width greater than about 20cm will lead to excessive losses of cell efficiency.

3.2.2 COST EFFECTIVENESS CONSIDERATIONS

Of course, the primary interest is not in cell efficiency alone but rather in the cost effective trade-offs involved in making cell size (ribbon width) larger at the expense of cell efficiency. As previously described, the impetus to increase cell size is the assumption that large area cells may be fabricated and processed more inexpensively than an equivalent silicon area comprised of smaller area cells. The cost effectiveness of losing cell efficiency while increasing cell size and reducing processing costs can be visualized by extending the example analysis presented above with a few basic assumptions about cost.

Assume first that the silicon cost per unit area is constant, independent of ribbon width W. The validity of this assumption is questionable since it is anticipated that the cost of silicon ribbon or sheet as a function of ribbon width will pass through a minimum making one width cheaper than others. As ribbon and sheet technologies mature, however, the basic cost of silicon will be a dominant factor, so the curve of ribbon cost vs. width will pass through a broad minimum, and the validity of this assumption is easily sufficient for this discussion. In addition, the cost per unit area of materials expended during cell and module fabrication and materials incorporated into the cell and encapsulation is also assumed constant. This assumption is expected to be generally valid. Therefore, a cell material cost per unit area, C_M, is

defined equal to silicon cost plus cell fabrication materials cost plus encapsulation materials cost.

Next assume that the processing cost per unit cell length is constant, independent of W. That is, cells of different widths, W, can be processed with identical throughputs and expense. In practice, it may not be possible to process very wide ribbons as inexpensively per unit length as narrow and moderate width ones. At any rate, a cell processing cost per unit length, C_P, is defined to include all costs other than materials, i.e., labor, depreciation, etc., for fabricating, interconnecting, and encapsulating cells. The cell processing cost per unit area then becomes C_P/W. Hence, the larger the ribbon width processed, the lower the net processing cost per unit area.

The total encapsulated solar cell cost per unit area, C_T, is now given by

$$C_T = C_M + \frac{C_P}{W} \quad , \tag{20}$$

the sum of materials and processing costs, where C_M and C_P are both constants. A relation between C_M and C_P can be determined by considering a baseline cell fabrication and encapsulation process. Let the 2cm wide ribbon detailed in the previous calculations serve as the baseline. Processing this material would be similar to fabricating 2cm x 2cm solar cells, and the costs of materials and processing for such cells are well known.

It is now necessary to assume some relation between the materials cost and the processing cost. Let k be defined as the ratio of materials cost per unit solar cell area to processing cost per unit area for the baseline W=2cm case. The value of k will be varied; but as a discussion point, a reasonable value for reference might be k=2, for which materials cost is 2/3, and processing cost is 1/3, of the total cost per unit area. Forming the ratio,

$$k = \left. \frac{C_M}{C_{P/W}} \right|_{W=2} = \frac{2\ C_M}{C_P} \tag{21}$$

Therefore,

$$C_P = \frac{2}{k} C_M \; . \tag{22}$$

As cell width increases beyond the baseline width, the total cost per unit area will decrease below the baseline cost value. Substituting equation (22) into equation (20) gives

$$C_T = C_M + \frac{1}{W}\left[\frac{2}{k} C_M\right] \tag{23}$$

$$= C_M \left[1 + \frac{2}{kW}\right] \; . \tag{24}$$

Equation (24) expresses the total cost per unit area as a function of cell with, W, and a given assumed value of k.

In considering cost tradeoffs, it is desirable to minimize the total cost per watt of power output. Thus, the total cost per unit area, C_T, should be divided by the output power density. An equivalent figure of merit is obtained by dividing C_T by cell efficiency η. Both C_T and η are functions of cell with W. From equation (24),

$$\frac{C_T\ (W)}{\eta\ (W)} = C_M \left[1 + \frac{2}{kW}\right] \frac{1}{\eta(W)} \; . \tag{25}$$

Values for η (W) may be obtained from the curves of Figures 4, 5, and 6. The parameter C_T (W)/η(W) can be expressed as a percentage of the constant C_M, the materials cost per unit area.

Equation (25) is plotted in Figure 7 for several values of k for the case of 10% metal coverage, 8 lines per 2cm ribbon segment length, ρ_m=.01Ω/□ , and ρ_S=40Ω/□ . For the reasonable value of k=2, the minimum cost per watt occurs for a ribbon width between 8 and 10cm. Other k values give different minima. For the more extreme case k=0.2, where processing costs are five times greater than materials costs (for 2cm width), the most cost-effective width is about 17cm. Note, however, that this case implies a higher cost per watt and a lower solar cell efficiency (as seen in Figure 4).

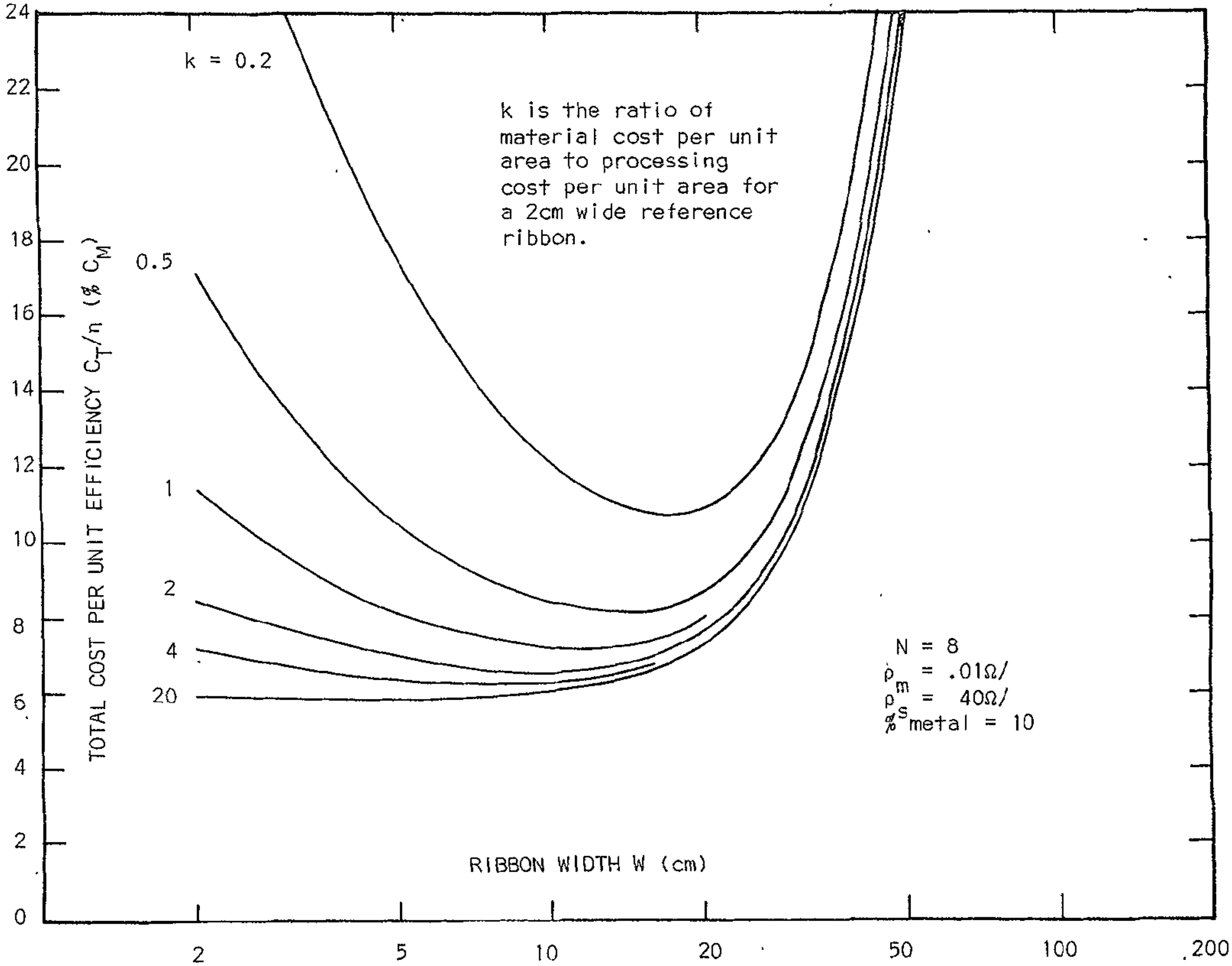

FIGURE 7: TOTAL COST PER UNIT EFFICIENCY (WHICH IS SIMILAR TO DOLLARS PER WATT) VERSUS RIBBON SUBSTRATE WIDTH. THIS IS SHOWN AS A FUNCTION THE RATIO OF MATERIAL COSTS TO PROCESSING COSTS FOR THE BASELINE CASE OF 2cm WIDE RIBBON.

It must be noted that as processes are developed to maturity and automated, the materials costs will be an increasing proportion of the total cost; the value of k will increase as a function of time. As the value of k increases, the most cost effective cell size decreases, but the sensitivity to cell size decreases below some maximum size. It should be observed that the parametric curves in Figure 7 were referenced to a 2cm cell width for an infinitely long cell. If, in fact, the reference cell had been assumed to be 20cm wide, the curve labeled k=1 would instead be labeled k=10. This in no way changes the concept that, regardless of chosen size, when materials costs become predominant over processing costs, the lower curves of Figure 7 (those having the highest values of the parameter k) show the limiting cost effectiveness of actual sizes. It is the projection here, that the optimum solar cell size will be less than 10cm. The attendant conclusion is that efforts to grow sheet greater than this size should not be pursued.

3.3 SELECTION OF PROCESSES AND PROCESS SEQUENCES

A solar cell is manufactured by a number of process steps which form a process sequence. As has been emphasized throughout this contract, there are many interactions between the individual process steps which must be considered in forming a process sequence.

Five process sequences which have a high probability of meeting the long range LSSA Project goals are presented in Tables 3 through 7.

The first process sequence, Table 3, utilizes only diffusion processes for junction formations; a planar p-n junction is produced. In this process sequence, one side of the substrate is texture etched while the other side is protected by a resist during texturing and hence remains flat. The texture-etched surface is then protected with an undoped spin-on (spray-on) silicon dioxide layer to mask against a boron diffusion on the back surface. Following back surface diffusion, the front surface is patterned to form the planar p-n junction area, followed by a phosphorous diffusion to form that junction. All dielectrics on the cell are now stripped, followed by deposition of a silicon-nitride layer to form the antireflection coating. At this point, two options exist. The first, and simpler, option is to pattern the cell front dielectric with the desired metallization pattern and strip the back surface dielectric. This is followed by a plated and solder coated metallization. The second option, if it is desired to obtain a deeper p-n junction under the contact metal, is to modify the sequence to add an additional phosphorus diffusion into the contact areas. While forming the front surface contact pattern, the back surface dielectric is protected, leaving it to serve as a diffusion mask. Following the contact enhancement diffusion, this back surface dielectric is stripped and the cell metallized.

The second process sequence, Table 4, combines diffusion and ion implantation steps to form junctions. A blanket p^+ boron diffusion is performed simultaneously

with the growth of an oxide layer. One side of the substrate is then protected while the other is stripped of oxide and texture etched. The substrate is then coated with a film of silicon nitride, which, among other functions, will ultimately act as the antireflection coating. The metallization pattern is formed by etching into the silicon nitride layer, simultaneously clearing the back surface. The substrate is then ion implanted to form the P-N junction, during which the edges of the substrate are mechanically masked so that the P-N junction will be planar. Implantation is performed such that peak dopant concentration occurs near the silicon-dielectric interface, enhancing the electric field configuration for improved carrier collection. Implantation into the contact areas is deeper and produces a higher concentration than in areas covered by silicon nitride, resulting in a deeper P-N junction depth beneath the metallization areas. After the next step of activation annealing, the cell is metallized by plating and soldering.

The third process sequence utilizes only ion implantation for junction formations, Table 5. As in the first sequence, the wafer is texture-etched on one side. Next, the silicon nitride antireflection coating is deposited, patterned on the front surface and stripped from the back surface. Two ion implantation steps follow: P^+ (boron) into the back surface and N^+ (phosphorus), again mechanically masked to form a planar junction, into the front surface. Both implants are simultaneously activated through an anneal, followed by metallization plating and solder coating.

The fourth process sequence, Table 6, is an all diffusion process sequence. A blanket P+ boron diffusion is performed on both sides of the silicon substrate, simultaneously growing a silicon dioxide layer. The wafer back is then protected, the front oxide removed, the resist removed, and the exposed silicon surface texture etched. A phosphorous diffusion is then performed into the textured front surface. Following this diffusion, the wafer is resisted, front and back, patterned on the front, and mesa etched on the substrate edge. The cell is then coated with an antireflection layer of silicon nitride, passivating the P-N junction. Next, the silicon nitride is etched in a photoresist step to form the front metallization pattern, while removing all dielectrics from the back surface. The cell is then metallized by plating and solder coating. This process sequence is more closely related to traditional solar cell manufacturing techniques and will be studied as a comparison baseline for the other process sequences.

The fifth process sequence, Table 7, is an all ion implanted (I^2) process sequence which differs from the sequence presented in Table 5 primarily in the order of the process steps. This difference, however, modifies the steps themselves dramatically. The sequence starts with a resist application to one side of the silicon substrate, the texture etching of the other side, and the removal of the resist. Following substrate cleaning, the wafer is first boron implanted on the back surface and then phosphorus implanted on the front through a mechanical mask to form the planar P-N junction. These implants do not pass through a dielectric film and, thus, must be performed at much lower voltages than in the sequence presented in Table 5 in which implants are performed through a dielectric film. Following implantation, an activation anneal is performed; this is followed by deposition of the silicon

TABLE 3: All diffusion process sequence resulting in planar type P-N junction. Option (b) is to increase P-N junction depth beneath metallization contacts.

1. Resist back, Texture front, strip resist
2. Spin-on oxide, front
3. P^+ (boron) diffusion (back)
4. Pattern front (protect back) to form planar pattern
5. Phosphorous diffusion to form planar P-N junction
6. Strip both surfaces, and AR coat (both surfaces) with dielectric (silicon nitride)

    (a) 7. Pattern front, strip back

    8. Metal

    (b) 7. Pattern front, protect back

    8. Phosphorous diffusion - contact area

    9. Strip back

    10. Metal

TABLE 4: Combined diffusion and ion implantation process sequence resulting in planar P-N junction.

1. P^+ (boron) diffusion, front and back, and oxide growth
2. Strip front and texture etch
3. AR coat - dielectric
4. Pattern front, strip back
5. I^2 front - phosphorous (planar)
6. Activation anneal
7. Metal

TABLE 5: All ion implanted process sequence with planar P-N junction.

1. Resist back, texture etch front, strip resist and clean
2. AR coat - dielectric
3. Pattern front, strip back
4. I^2 back - boron
5. I^2 front - phosphorous (planar)
6. Activation anneal
7. Metal

TABLE 6:

ALL DIFFUSION PROCESS INCORPORATING PASSIVATED MESA-ETCHED P-N JUNCTION PERIMETER

1. P+ (boron) diffusion, front and back, and oxide growth.
2. Strip front and texture etch.
3. Phosphorus diffusion
4. Mesa Etch
5. AR coat-dielectric
6. Pattern front, strip back
7. Metal

TABLE 7

ALL ION IMPLANTATION PROCESS WITH PLANAR JUNCTION. BARE SILICON SURFACE IMPLANTATION.

1. Resist back, texture etch front, strip resist and clean.
2. I^2 back - boron.
3. I^2 front - phosphorus (planar)
4. Activation Anneal
5. AR coat - dielectric
6. Pattern front, strip back.
7. Metal

nitride antireflection coating. The antireflection coating is then patterned during a photoresist step to form the front metal pattern and to clear dielectric from the back surface. The cell is then metallized and solder coated.

The five process sequences which have now been presented are comprised of many common process steps. In some cases, a process step may be performed by several different techniques. A summary of distinct process steps which are being analyzed during this study is shown in Table 8.

3.4 DEFINITION OF PRIMARY PROCESS VARIABLES

Each of the process steps in Table 8 can be utilized in a satisfactory process sequence. Accordingly, to facilitate choice of an optimized process sequence, it is necessary that process variables be defined for each step in order to specify the details and control limits for each. This study is centered around the primary process variables, which, like solar cell variables, are those variables which can be controlled by the operator before and during performance of a process, while diagnostic variables are those variables which are measured after completion of a process step to determine changes effected by the step. In some cases, these diagnostic variables will also be the same as solar cell variables.

In order to effectively study the interaction of process and cell variables, some process variables may be specified in a process step definition. For example, a phosphorus diffusion could be performed from a variety of sources, the type of source being considered a variable. This could lead to a nearly infinite study matrix. To maintain a manageable study, one phosphorus source, phosphine (PH_3), will be "defined" as part of the process step for a phosphorus diffusion. This will increase the effectiveness of

TABLE 8:

PROCESS STEPS AND OPTIONS FOR INCLUSION IN PROCESS SEQUENCES BEING STUDIED

1. Patterning Operations
    a. Photoresist Application
        1. Spin
        2. Spray
    b. Photoresist Removal
        1. Wet Chemistry
        2. Plasma
    c. Photoresist alignment, exposure, development
        1. Spray development
        2. Immersion development
    d. Ion implantation shadow masking
2. Etching Operations
    a. Dielectric etching
        1. Wet Chemistry
        2. Plasma
    b. Silicon etching
        1. Wet Chemistry
        2. Plasma
    c. Texture etching
3. Cleaning Operations
    a. Wet Chemistry
    b. Centrifuge rinsing and drying
    c. Plasma
    d. Scrubbing
4. Dielectric Deposition
    a. Silicon nitride
    b. Spin-on (Spray-on) Oxide
5. Doping Operations
    a. Diffusion
        1. Boron
        2. Phosphorus
        3. Arsenic

TABLE 8: (continued)

b. Ion Implantation

1. Boron

2. Phosphorus

3. Arsenic

c. Annealing (activation)

6. Metallization

a. Plating

b. Sintering

c. Solder Coating

this study by allowing more attention to variables of processing which can be controlled by the process operator. Similar situations may exist for other process steps, and choices will be made to limit the scope of the study. Of course, considerable judgment must be exercised in such choices to guarantee that the selected process is at least near optimal for performance of the particular function.

The following tables (9 through 24) define the primary process variables for the chosen process steps. Where variables are common, processes have been grouped together for ease of presentation.

TABLE 9:

PROCESS VARIABLES FOR PHOTORESIST
APPLICATION AND SPIN-ON OXIDE APPLICATION

OPERATIONAL VARIABLES

SPINNING	SPRAYING
Spin speeds	Pressure
Application Sequences	Nozzle Configuration
	Table Speed
	Application Sequences

Type of Resist or Spin-on Material

Viscosity

Dispense time and amount

Preparation of Surface

Bake time, temperature, heat source, and ambient

Substrate surface quality and texture

Wafer carrier: Capacity, configuration, thermal mass

DIAGNOSTIC VARIABLES

Coverage thickness

Coating uniformity

Adherence

Etch resistance

Index of refraction (oxide)

TABLE 10:

PROCESS VARIABLES FOR PHOTORESIST REMOVAL

OPERATIONAL VARIABLES

PLASMA	WET CHEMISTRY
Gas Composition	Chemical Composition
Gas Pressure	Temperature
Gas Flow Rate	Time
Gas Flow Pattern	Spacing
RF Power and Frequency	Agitation
Time	Rinse Cycle(s)
Chamber Size	Bath Size
Chamber Geometry	

DIAGNOSTIC VARIABLES

Visible Residue

Contamination, e.g., metallic ion residues

TABLE 11:

PROCESS VARIABLES FOR PHOTORESIST ALIGNMENT, EXPOSURE, AND DEVELOPMENT

OPERATIONAL VARIABLES

Type of process (proximity, projection, contact)
Variations in substrate dimensions
Thickness of photoresist
Substrate positioning
Mask type
Light intensity and uniformity
Exposure time
Surface quality
Development Method:
    Spray -- pressure and nozzle configuration
    Immersion -- agitation

Development Time

Developer Temperature
Developer composition
Rinsing and drying cycles
Bake time, temperature, and ambient

DIAGNOSTIC VARIABLES

Pattern dimensions
Pattern location
Pattern integrity
Completeness of pattern development

TABLE 12:

PROCESS VARIABLES FOR ION IMPLANTATION SHADOW MASKING

OPERATIONAL VARIABLES

Variations in silicon dimensions

Mask and holder design and tolerances

Material of mask construction
(knock-on impurities)

DIAGNOSTIC VARIABLES

Pattern (junction edge) position

TABLE 13:

PROCESS VARIABLES FOR WET ETCHING AND CLEANING OF DIELECTRICS AND SILICON

OPERATIONAL VARIABLES

- Dielectric or silicon characteristics
  - (Thickness, doping, composition, etch rate, stain, etc.)
- Bath composition and purity of chemicals
- Bath temperature
- Time of etching (and end point determination)
- Agitation
- Bath size, life, and loading factors
- Substrate preparation
- Substrate rinsing
- Wafer carrier: spacing, load

DIAGNOSTIC VARIABLES

- Adequate removal criteria
- Pattern definition (if applicable)

TABLE 14:

PROCESS VARIABLES FOR PLASMA ETCHING AND CLEANING OF DIELECTRICS AND SILICON

OPERATIONAL VARIABLES

Dielectric or silicon characteristics
(Thickness, doping, composition, etch rate, strain)

Gas composition and purity

Gas flow rates and pressure

Substrate spacing

RF power and frequency

Etch and cleaning cycle times

Chamber size

End point detection

DIAGNOSTIC VARIABLES

Adequate removal criteria

Pattern definition (if applicable)

TABLE 15:

PROCESS VARIABLES FOR TEXTURE ETCHING

OPERATIONAL VARIABLES

Bath composition

Bath temperature

Etching time

Purity of chemicals

Substrate starting surface
(mechanical condition and doping level)

Agitation

Bath size, life, and loading factors

DIAGNOSTIC VARIABLES

Completeness criteria

Quality and uniformity of texturing

TABLE 16:

PROCESS VARIABLES FOR CENTRIFUGE
RINSING AND DRYING

OPERATIONAL VARIABLES

Spin speed

Time

Temperature

Water pressure and purity

Gas pressure, purity, and type

Loading and balancing factors

DIAGNOSTIC VARIABLES

Completeness of drying

Filming or spotting by residues

TABLE 17:

PROCESS VARIABLES FOR HIGH PRESSURE SCRUBBING

OPERATIONAL VARIABLES

Pressure

Water purity

Nozzle configuration

Time

Dry spin-speed

DIAGNOSTIC VARIABLES

Cleanliness criteria

TABLE 18:

PROCESS VARIABLES FOR DIELECTRIC DEPOSITION
(e.g., LOW PRESSURE CHEMICAL VAPOR DEPOSITION OF SILICON NITRIDE)

OPERATIONAL VARIABLES

- Reactor temperature and temperature profile
- Reactor geometry
- Substrate configuration in reactor
- Sequence and time of cycles
- RF energy (if used)
- Gas compositions and purities
- Pressure
- Substrate surface preparation

DIAGNOSTIC VARIABLES

- Film thickness
- Film index of refraction
- Uniformity:
  - across substrate
  - throughout reactor

TABLE 19:

PROCESS VARIABLES FOR DOPING BY DIFFUSION
(Selected source such as PH_3, BCl_3)

OPERATIONAL VARIABLES

Furnace temperature and profile

Time, including portions of the cycle start and finish.

Gas mixture(s) and flow rates

Gas purities

Furnace tube size

Furnace cleanliness

Substrate spacing and orientation to gas flow

Insertion transients

Removal transients

DIAGNOSTIC VARIABLES

On a test wafer:

sheet resistivity

junction depth

oxide thickness and index of refraction

bulk lifetime

surface layer lifetime

Uniformity: across substrate, down furnace length

TABLE 20:

PROCESS VARIABLES FOR ION IMPLANTATION DOPING

OPERATIONAL VARIABLES

- Dopant species
- Voltage (or voltages)
- Analysis quality
- Beam currents and times: dose levels
- Beam power density (heating); substrate temperature
- Substrate surface quality
- Substrate crystal orientation (channeling)
- Dielectric surface layer species and thickness
- Surface angle

DIAGNOSTIC VARIABLES

On a test wafer after activation annealing:

- Sheet resistivity
- Junction depth
- Uniformity over a substrate
- Uniformity substrate-to-substrate
- Bulk lifetime
- Surface layer lifetime

TABLE 2.1:

PROCESS VARIABLES FOR ACTIVATION ANNEALING

<u>OPERATIONAL VARIABLES</u>

- Temperature
- Time and heating rate
- Dose, species, and energy of implant
- Ambient gas(es) and flow rates
- Substrate spacing
- Wafer carrier: size, capacity, thermal mass

<u>DIAGNOSTIC VARIABLES</u>

- Sheet resistivity
- Junction depth
- Uniformity over a substrate
- Uniformity substrate-to-substrate
- Bulk lifetime
- Surface lifetime

TABLE 22:

PROCESS VARIABLES FOR PLATING

OPERATIONAL VARIABLES

- Bath composition and purity of components
- Bath temperature
- Immersion time
- Agitation
- Substrate dopant type and level
- Bath size, life, and loading factors
- Substrate spacing
- Substrate surface preparation
- Substrate rinsing time and temperature
- Drying process

DIAGNOSTIC VARIABLES

- Metal thickness and uniformity
- Metal series resistance
- Metal-silicon contact resistance
- Adhesion
- Uniformity of subsequent solder coating

TABLE 23:

PROCESS VARIABLES FOR METALLIZATION SINTERING

OPERATIONAL VARIABLES

- Temperature
- Times of sequences for cycle
- Ambient gas and gas flow rate
- Substrate spacing
- Wafer carrier, size, capacity, thermal mass

DIAGNOSTIC VARIABLES

- Metal adherence (pull test)
- Metal penetration into silicon
- Contact resistance
- Photovoltaic parameters (I_{sc}, V_{oc}, F.F., R_{sh}, R_s)
- Color changes (if silicides or oxides form)
- Uniformity of subsequent solder coating

TABLE 24:

PROCESS VARIABLES FOR SOLDER COATING

<u>OPERATIONAL VARIABLES</u>

- Solder composition
- Flux
- Dross inhibitor
- Temperature of solder
- Time in solder
- Method of substrate support
- Contamination and bath life
- Cleaning solution(s)

<u>DIAGNOSTIC VARIABLES</u>

- Uniformity and thickness of solder coating
- Series resistance of solar cell
- Solar cell cleanliness

3.5 RELATIONSHIPS BETWEEN PRIMARY PROCESS VARIABLES AND CELL VARIABLES

The primary process variables listed in Tables 9 through 24 are related, in varying degrees, to the primary solar cell variables listed in Tables 1 and 2. In fact, it is recognized that nearly all of the cell variables and process variables are interrelated, so that changing any one will affect many others.

The direct and indirect relations between primary process variables and primary cell variables are presented, in a qualitative fashion, in Tables 25 through 41. Each of these tables is separated into two portions, A and B, with the "A" tables relating primary process variables (both operational and diagnostic) to primary solar cell operational variables and the "B" tables relating the same process variables to the solar cell diagnostic variables.

For each of these tables, the following key is used:

X Strong or direct relationship

(X) Weak or indirect relationship

* Primary process variable and solar cell variable are the same, by definition.

Definitions of the terms for the solar cell variables are listed in Tables 1 and 2.

Since nearly all of the designated variables are interrelated, showing such relations on these tables would result in the tables being mostly filled, reducing their usefulness. Accordingly, entries on the tables are restricted to the several variables most strongly affected and those which would most readily and likely be evaluated for changes.

There are several judgements to be exercised in determining whether a relationship between a process variable and a solar cell variable is direct, indirect, or sufficiently remote that the interaction would be noted only

TABLE 25A:
VARIABLES FOR PHOTORESIST APPLICATION

	OPERATIONAL SOLAR CELL VARIABLES																			
	I_{sc}	V_{oc}	P_{max}	η	$V_{P_{max}}$	$I_{P_{max}}$	FF	R_{series}	R_{shunt}	t	D	L	W	A	A_j	A_M	$(A_M/A_j) \times 100\%$	t_M	W_M	L_M
OPERATIONAL PROCESS VARIABLES																				
SPINNING																				
Spin Speeds											X	X	X							
Application Sequences														(X)						
SPRAYING																				
Pressure																				
Nozzle Configuration											X	X	X							
Table Speed											X	X	X							
Application Sequences														(X)						
Type of Resist																				
Viscosity																				
Dispense time and amount														X						
Bake time, temperature, heat source, and ambient																				
Substrate surface quality and texture																				
DIAGNOSTIC PROCESS VARIABLES																				
Coverage thickness																			(X)	(X)
Coating uniformity																				
Adherence																				
Etch resistance																				

TABLE 25B:
VARIABLES FOR PHOTORESIST APPLICATION

	DIAGNOSTIC SOLAR CELL VARIABLES																				
	x_j	x_m	ρ_s	ρ_{sm}	ρ_s back	X_j back	ρ	C_s	C_s back	$C(x)$	$C(x)$ back	(hkl)	$N_\perp$	$I_{SC}(\lambda)$	τ	I vs V	S	$R(\lambda)$	W_B	μ	Uniform
<u>OPERATIONAL PROCESS VARIABLES</u>																					
<u>SPINNING</u>																					
Spin Speeds																					(X)
Application Sequences																					
<u>SPRAYING</u>																					
Pressure																					(X)
Nozzle Configuration																					(X)
Table Speed																					(X)
Application Sequences																					
Type of Resist															(X)		(X)				
Viscosity																					(X)
Dispense time and amount																					(X)
Bake time, temperature, heat source and ambient															(X)		(X)				X
Substrate surface quality and texture																					
<u>DIAGNOSTIC PROCESS VARIABLES</u>																					
Coverage thickness																					X
Coating uniformity																					*
Adherence																					
Etch resistance																					

TABLE 26A:
VARIABLES FOR MASKING SPIN-ON OXIDE APPLICATION

	OPERATIONAL SOLAR CELL VARIABLES																			
	I_{sc}	V_{oc}	P_{max}	η	$V_{P_{max}}$	$I_{P_{max}}$	FF	R_{series}	R_{shunt}	t_j	D	L	W	A	A_j	A_M	$(A_M/A_j) \times 100\%$	t_M	W_M	L_M
OPERATIONAL PROCESS VARIABLES																				
SPINNING																				
Spin Speeds											X	X	X							
Application Sequences														(X)						
SPRAYING																				
Pressure																				
Nozzle Configuration											X	X	X							
Table Speed											X	X	X							
Application Sequences														(X)						
Viscosity																				
Dispense time and amount														(X)						
Preparation of surface																				
Bake time, temperature, heat source, and ambient																				
Substrate surface quality and texture																				
DIAGNOSTIC PROCESS VARIABLES																				
Coverage thickness																				
Coating uniformity																				
Adherence																				
Index of refraction																				

TABLE 26B:
VARIABLES FOR MASKING SPIN-ON OXIDE APPLICATION

	DIAGNOSTIC SOLAR CELL VARIABLES																				
	x_j	x_m	ρ_s	ρ_{sm}	ρ_s back	X_j back	ρ	C_s	C_s back	$C(x)$	$C(x)$ back	(hkl)	$N_\perp$	$I_{SC}(\lambda)$	τ	I vs V	S	$R(\lambda)$	W_B	M	Uniform
<u>OPERATIONAL PROCESS VARIABLES</u>																					
<u>SPINNING</u>																					
Spin Speeds																					(X)
Application Sequences																					
<u>SPRAYING</u>																					
Pressure																					(X)
Nozzle Configuration																					(X)
Table Speed																					(X)
Application Sequences																					
Viscosity																					(X)
Dispense time and amount																					(X)
Preparation of surface																	(X)				(X)
Bake time, temperature, heat source, and ambient															(X)		(X)				
Substrate surface quality and texture																					X
<u>DIAGNOSTIC PROCESS VARIABLES</u>																					
Coverage thickness																					X
Coating uniformity																					*
Adherence																					X
Index of refraction																					

TABLE 27A:
VARIABLES FOR PHOTORESIST REMOVAL

	OPERATIONAL SOLAR CELL VARIABLES																			
	I_{sc}	V_{oc}	P_{max}	η	$V_{P max}$	$I_{P max}$	FF	R_{series}	R_{shunt}	t	D	L	W	A	A_j	A_M	$(A_M/A_j) \times 100\%$	t_M	W_M	L_M
OPERATIONAL PROCESS VARIABLES																				
PLASMA																				
Gas Composition	(X)						(X)													
Gas Pressure																				
Gas Flow Rate																				
Gas Flow Pattern																				
RF Power and Frequency																				
Time																				
Spacing																				
Chamber Size											X	X	X	(X)						
Chamber Geometry											X	X	X	(X)						
WET CHEMISTRY																				
Chemical Composition	(X)						(X)													
Temperature																				
Time																				
Spacing																				
Agitation																				
Rinse Cycle(s)																				
Bath Size											X	X	X	(X)						
DIAGNOSTIC PROCESS VARIABLES																				
Visible Residue	X	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)											
Contamination, e.g., metallic ion residues	(X)	X	(X)	(X)	(X)	(X)	X	(X)	X											

TABLE 27B:
VARIABLES FOR PHOTORESIST REMOVAL

	DIAGNOSTIC SOLAR CELL VARIABLES																				
	x_j	x_m	ρ_s	ρ_{sm}	ρ_s back	X_j back	ρ	C_s	C_s back	$C(x)$	$C(x)$ back	(hkl)	$N_\perp$	$I_{SC}(\lambda)$	τ	I vs V	S	$R(\lambda)$	W_B	ℓ	Uniform
OPERATIONAL PROCESS VARIABLES																					
PLASMA																					
Gas Composition													(X)		(X)		(X)				
Gas Pressure																					X
Gas Flow Rate																					X
Gas Flow Pattern																					X
RF Power and Frequency																					
Time																					
Spacing																					X
Chamber Size																					
Chamber Geometry																					
WET CHEMISTRY																					
Chemical Composition													(X)		(X)		(X)				
Temperature																					
Time																					
Spacing																					X
Agitation																					X
Rinse Cycle(s)															(X)		(X)				
Bath Size																					
DIAGNOSTIC PROCESS VARIABLES																					
Visible Residue														X	(X)	(X)	(X)			X	
Contamination, e.g., metallic ion residues														(X)	X	(X)	X			X	

TABLE 28A:
VARIABLES FOR PHOTORESIST ALIGNMENT, EXPOSURE, AND DEVELOPMENT

	OPERATIONAL SOLAR CELL VARIABLES																			
	I_{sc}	V_{oc}	P_{max}	η	$V_{P max}$	$I_{P max}$	FF	R_{series}	R_{shunt}	t	D	L	W	A	A_j	A_M	$(A_M/A_j) \times 100\%$	t_M	W_M	L_M
OPERATIONAL PROCESS VARIABLES																				
Type of process (proximity, projection, contact)																			(X)	(X)
Variations in substrate dimensions															(X)	(X)				
Thickness of photoresist																				
Substrate positioning																				
Mask type																				
Light intensity and uniformity																				
Exposure time																				
Surface quality																				
Development Method:																				
Spray — pressure and nozzle configuration																				
Immersion — agitation																				
Development time																				
Developer temperature																				
Developer composition																				
Rinsing and drying cycles	(X)						(X)		(X)											
Bake time, temperature, and ambient	(X)						(X)		(X)											
DIAGNOSTIC PROCESS VARIABLES																				
Pattern dimensions											(X)	(X)	(X)		(X)	(X)	(X)		X	X
Pattern location									(X)											
Pattern integrity					(X)	(X)		(X)	(X)											
Completeness of pattern development	(X)	(X)					(X)	(X)	(X)						(X)	(X)				

TABLE 28B:
VARIABLES FOR PHOTORESIST ALIGNMENT, EXPOSURE, AND DEVELOPMENT

	DIAGNOSTIC SOLAR CELL VARIABLES																				
	x_j	x_m	ρ_s	ρ_{sm}	ρ_s back	X_j back	ρ	C_s	C_s back	$C(x)$	$C(x)$ back	(hkl)	$N_\perp$	$I_{SC}(\lambda)$	τ	I vs V	S	$R(\lambda)$	W_B	η	Uniform
OPERATIONAL PROCESS VARIABLES																					
Type of process (proximity, projection, contact)																					X
Variations in substrate dimensions																			(X)		X
Thickness of photoresist																					(X)
Substrate positioning																					
Mask type																					
Light intensity and uniformity																					X
Exposure time																					
Surface quality																					(X)
Development method:																					
Spray -- pressure and nozzle configuration																					
Immersion -- agitation																					
Development time																					
Developer temperature																					
Developer composition																					
Rinsing and drying cycles															(X)		(X)				
Bake time, temperature, and ambient															(X)		(X)				
DIAGNOSTIC PROCESS VARIABLES																					
Pattern dimensions																					
Pattern location																					
Pattern integrity																					(X)
Completeness of pattern development																					X

FIGURE 29A:
VARIABLES FOR ION IMPLANTATION SHADOW MASKING

	OPERATIONAL SOLAR CELL VARIABLES																			
	I_{sc}	V_{oc}	P_{max}	η	$V_{P_{max}}$	$I_{P_{max}}$	FF	R_{series}	R_{shunt}	t	D	L	W	A	A_j	A_M	$(A_M/A_j) \times 100\%$	t_M	W_M	L_M
OPERATIONAL PROCESS VARIABLES																				
Variations in silicon dimensions										*	*	*	*	*						
Mask and holder design and tolerances	X		(X)	(X)		(X)				X	X	X	X	X	X		(X)			
Material of Mask Construction (knock-on impurities)	X	X	(X)	(X)	(X)	(X)	X		X											
DIAGNOSTIC PROCESS VARIABLES																				
Pattern (Junction edge) position	X		(X)	(X)		(X)			(X)		X	X	X	X	X		(X)			

TABLE 29B:
VARIABLES FOR ION IMPLANTATION SHADOW MASKING

	DIAGNOSTIC SOLAR CELL VARIABLES																			
	x_j	x_m	ρ_s	ρ_{sm}	ρ_s back	X_j back	ρ	C_s	C_s back	C (x)	C (x) back	(hkl)	$N_\perp$	I_{SC} (λ)	τ	I vs V	S	R (λ)	W_B	M	Uniform
<u>OPERATIONAL PROCESS VARIABLES</u>																					
Variations in silicon dimensions																					X
Mask and holder design and tolerances																(X)					
Material of Mask Construction (knock-on impurities)														X	X	X	(X)				
<u>DIAGNOSTIC PROCESS VARIABLES</u>																					
Pattern (Junction edge) position																(X)					

TABLE 30A:
VARIABLES FOR WET ETCHING AND CLEANING OF DIELECTRICS AND SILICON

	OPERATIONAL SOLAR CELL VARIABLES																			
	I_{sc}	V_{oc}	P_{max}	η	$V_{P_{max}}$	$I_{P_{max}}$	FF	R_{series}	R_{shunt}	t	D	L	W	A	A_j	A_M	$(A_M/A_j) \times 100\%$	t_M	W_M	L_M
OPERATIONAL PROCESS VARIABLES																				
Dielectric or Silicon Characteristics (Thickness, doping, composition, etch rate, strain, etc.)	X	X	(X)	(X)	(X)	(X)	X									(X)	(X)	(X)	X	X
Bath composition and purity of chemicals	(X)	(X)					(X)	(X)	(X)											
Bath temperature	(X)	(X)																		
Time of etching (and end point determination)	(X)	(X)													(X)	(X)				
Agitation	(X)	(X)									X	X	X	(X)	(X)	(X)				
Bath size, life, and loading factors	(X)	(X)									(X)	(X)	(X)	X	X	X				
Substrate preparation																				
Substrate rinsing							(X)	(X)	(X)											
DIAGNOSTIC PROCESS VARIABLES																				
Adequate removal criteria	(X)	(X)					(X)	(X)	(X)											
Pattern definition (if applicable)																(X)	(X)	(X)	X	X

DIAGNOSTIC SOLAR CELL VARIABLES

TABLE 30B:
VARIABLES FOR WET ETCHING AND CLEANING OF DIELECTRICS AND SILICON

	x_j	x_m	ρ_s	ρ_{sm}	ρ_s back	X_j back	ρ	C_s	C_s back	$C(x)$	$C(x)$ back	(hkl)	$N_\perp$	$I_{SC}(\lambda)$	τ	I vs V	S	$R(\lambda)$	W_B	M	Uniform
<u>OPERATIONAL PROCESS VARIABLES</u>																					
Dielectric or Silicon characteristics (Thickness, doping, composition, etch rate, strain, etc.)														X		X	(X)	X			X
Bath composition and purity of chemicals															(X)	(X)	(X)	(X)			
Bath temperature																		(X)			
Time of etching (and end point determination)																		(X)			(X)
Agitation																		(X)			X
Bath size, life, and loading factors																					(X)
Substrate preparation																					X
Substrate rinsing																					
<u>DIAGNOSTIC PROCESS VARIABLES</u>																					
Adequate removal criteria																					
Pattern definition (if applicable)																					(X)

TABLE 31A:
VARIABLES FOR PLASMA ETCHING AND CLEANING OF DIELECTRICS AND SILICON

	OPERATIONAL SOLAR CELL VARIABLES																			
	I_{sc}	V_{oc}	P_{max}	η	$V_{P_{max}}$	$I_{P_{max}}$	FF	R_{series}	R_{shunt}	t	D	L	W	A	A_j	A_M	$(A_M/A_j) \times 100\%$	t_M	W_M	L_M
OPERATIONAL PROCESS VARIABLES																				
Dielectric or Silicon Characteristics (Thickness, doping, composition, etch rate, strain, etc.)	X	X	(X)	(X)	(X)	(X)	X									(X)	(X)	(X)	X	X
Gas composition and purity	(X)	X					X	X	X											
Gas flow rates and pressure	(X)	(X)																		
Substrate spacing	(X)	(X)								(X)	X	X	X	X						
RF power and frequency	(X)	(X)												(X)	X	X				
Etch and cleaning cycle times	(X)	(X)									(X)	(X)	(X)	(X)	X	X				
Chamber size	(X)	(X)									X	X	X	(X)						
End point detection	(X)	(X)													(X)	(X)				
DIAGNOSTIC PROCESS VARIABLES																				
Adequate removal criteria	(X)	(X)					(X)	(X)	(X)											
Pattern definition (if applicable)																(X)	(X)	(X)	X	X

TABLE 31B:
VARIABLES FOR PLASMA ETCHING AND CLEANING OF DIELECTRICS AND SILICON

	DIAGNOSTIC SOLAR CELL VARIABLES																				
	x_j	x_m	ρ_s	ρ_{sm}	ρ_s back	X_j back	ρ	C_s	C_s back	$C(x)$	$C(x)$ back	(hkl)	$N_\perp$	$I_{SC}(\lambda)$	τ	I vs V	S	$R(\lambda)$	W_B	M	Uniform
OPERATIONAL PROCESS VARIABLES																					
Dielectric or Silicon Characteristics (Thickness, doping, composition, etch rate, strain, etc.)														X		X	(X)	X			X
Gas composition and purity															(X)	(X)	(X)	(X)			
Gas flow rates and pressure																					(X)
Substrate spacing																					(X)
RF power and frequency																		(X)			
Etch and cleaning cycle times															(X)	(X)	(X)				
Chamber size																					(X)
End point detection																		(X)			
DIAGNOSTIC PROCESS VARIABLES																					
Adequate removal criteria																					
Pattern definition (if applicable)																					(X)

TABLE 32A:
VARIABLES FOR TEXTURE ETCHING

	OPERATIONAL SOLAR CELL VARIABLES																			
	I_{sc}	V_{oc}	P_{max}	η	$V_{P_{max}}$	$I_{P_{max}}$	FF	R_{series}	R_{shunt}	t	D	L	W	A	A_j	A_M	$(A_M/A_j) \times 100\%$	t_M	W_M	L_M
OPERATIONAL PROCESS VARIABLES																				
Bath composition	(X)																			
Bath temperature	(X)																			
Etching time	(X)																			
Purity of chemicals							(X)		(X)											
Substrate starting surface (mechanical condition and doping level)																				
Agitation											X	X	X	(X)						
Bath size, life, and loading factors											X	X	X	X						
DIAGNOSTIC PROCESS VARIABLES																				
Completeness criteria	X														(X)					
Quality and uniformity of texturing	(X)														(X)					

TABLE 32B:
VARIABLES FOR TEXTURE ETCHING

	DIAGNOSTIC SOLAR CELL VARIABLES																				
	x_j	x_m	ρ_s	ρ_{sm}	ρ_s back	X_j back	ρ	C_s	C_s back	$C(x)$	$C(x)$ back	(hkl)	$N_\perp$	$I_{SC}(\lambda)$	τ	I vs V	S	$R(\lambda)$	W_B	M	Uniformi
OPERATIONAL PROCESS VARIABLES																					
Bath composition														(X)			(X)	X			
Bath temperature														(X)				(X)			
Etching time														(X)				(X)			
Purity of chemicals															(X)		(X)				
Substrate starting surface (mechanical condition and doping level)												X	(X)								X
Agitation																					(X)
Bath size, life, and loading factors																					
DIAGNOSTIC PROCESS VARIABLES																					
Completeness criteria												X						X			X
Quality and uniformity of texturing												X						(X)			X

TABLE 33A:
VARIABLES FOR CENTRIFUGE RINSING AND DRYING

	OPERATIONAL SOLAR CELL VARIABLES																			
	I_{sc}	V_{oc}	P_{max}	η	$V_{P_{max}}$	$I_{P_{max}}$	FF	R_{series}	R_{shunt}	t	D	L	W	A	A_j	A_M	$(A_M/A_j) \times 100\%$	t_M	W_M	L_M
<u>OPERATIONAL PROCESS VARIABLES</u>																				
Spin speed																				
Time																				
Temperature																				
Water pressure and purity							(X)		(X)											
Gas pressure, purity, and type										X	X	X	X	(X)						
Loading and balancing factors																				
<u>DIAGNOSTIC PROCESS VARIABLES</u>																				
Completeness of drying																				
Filming or spotting by residues	(X)						(X)		(X)											
Breakage of substrates										X	(X)	(X)	(X)							

TABLE 33B:
VARIABLES FOR CENTRIFUGE RINSING AND DRYING

DIAGNOSTIC SOLAR CELL VARIABLES

	x_j	x_m	ρ_s	ρ_{sm}	ρ_s back	X_j back	ρ	C_s	C_s back	$C(x)$	$C(x)$ back	(hkl)	N_L	$I_{SC}(\lambda)$	τ	I vs V	S	$R(\lambda)$	W_B	η	Uniform
<u>OPERATIONAL PROCESS VARIABLES</u>																					
Spin speed																					
Time																					
Temperature																					
Water pressure and purity															(X)		(X)				
Gas pressure, purity, and type																					
Loading and balancing factors																					
<u>DIAGNOSTIC PROCESS VARIABLES</u>																					
Completeness of drying																					X
Filming or spotting by residues														(X)	(X)		(X)				X
Breakage of substrates																					

TABLE 34A:
VARIABLES FOR HIGH PRESSURE SCRUBBING

	OPERATIONAL SOLAR CELL VARIABLES																			
	I_{sc}	V_{oc}	P_{max}	η	$V_{P_{max}}$	$I_{P_{max}}$	FF	R_{series}	R_{shunt}	t	D	L	W	A	A_j	A_M	$(A_M/A_j) \times 100\%$	t_M	W_M	L_M
<u>OPERATIONAL PROCESS VARIABLES</u>																				
Pressure																				
Water purity							(X)		(X)											
Nozzle configuration																				
Time											(X)	(X)	(X)	(X)						
Dry spin-speed											(X)	(X)	(X)	(X)						
<u>DIAGNOSTIC PROCESS VARIABLES</u>																				
Cleanliness criteria	(X)	(X)					(X)		(X)											

TABLE 34B:
VARIABLES FOR HIGH PRESSURE SCRUBBING

	DIAGNOSTIC SOLAR CELL VARIABLES																				
	x_j	x_m	ρ_s	ρ_{sm}	ρ_s back	X_j back	ρ	C_s	C_s back	$C(x)$	$C(x)$ back	(hkl)	N_L	$I_{SC}(\lambda)$	τ	I vs V	S	$R(\lambda)$	W_B	M	Uniformity
<u>OPERATIONAL PROCESS VARIABLES</u>																					
Pressure																					
Water purity															(X)		(X)				
Nozzle configuration																					
Time																					(X)
Dry spin-speed																					(X)
<u>DIAGNOSTIC PROCESS VARIABLES</u>																					
Cleanliness criteria															(X)	(X)	(X)				(X)

TABLE 35A:
VARIABLES FOR DIELECTRIC DEPOSITION
(e.g., LOW PRESSURE CHEMICAL VAPOR DEPOSITION
OF SILICON NITRIDE)

	OPERATIONAL SOLAR CELL VARIABLES																			
	I_{sc}	V_{oc}	P_{max}	η	$V_{P_{max}}$	$I_{P_{max}}$	FF	R_{series}	R_{shunt}	t	D	L	W	A	A_j	A_M	$(A_M/A_j) \times 100\%$	t_M	W_M	L_M
OPERATIONAL PROCESS VARIABLES																				
Reactor temperature and temperature profile	(X)	(X)																		
Reactor geometry											(X)	(X)	(X)	(X)						
Substrate configuration in reactor											(X)	(X)	(X)	(X)						
Sequence and time of cycles																				
RF energy (if used)																				
Gas compositions and purities							(X)		(X)											
Pressure																				
Substrate surface preparation	(X)																			
DIAGNOSTIC PROCESS VARIABLES																				
Film thickness	X	(X)				(X)														
Film index of refraction	X	(X)				(X)														
Uniformity:																				
across substrate	(X)										(X)	(X)	(X)	(X)						
throughout reactor	(X)													(X)						

TABLE 35B:
VARIABLES FOR DIELECTRIC DEPOSITION
(e.g., LOW PRESSURE CHEMICAL VAPOR DEPOSITION
OF SILICON NITRIDE)

DIAGNOSTIC SOLAR CELL VARIABLES

	x_j	x_m	ρ_s	ρ_{sm}	ρ_s back	X_j back	ρ	C_s	C_s back	$C(x)$	$C(x)$ back	(hkl)	$N_\perp$	$I_{SC}(\lambda)$	τ	I vs V	S	$R(\lambda)$	W_B	M	Uniformi
<u>OPERATIONAL PROCESS VARIABLES</u>																					
Reactor temperature and temperature profile	(X)					(X)		(X)	(X)	(X)	(X)					(X)					(X)
Reactor geometry																					(X)
Substrate configuration in reactor																					(X)
Sequence and time of cycles																					
RF energy (if used)																					
Gas compositions and purities															X		X				
Pressure																					(X)
Substrate surface preparation																					(X)
<u>DIAGNOSTIC PROCESS VARIABLES</u>																					
Film thickness														X				X			
Film index of refraction														X				X			
Uniformity:																					*
across substrate																					*
throughout reactor																					

TABLE 36A:
VARIABLES FOR DOPING BY DIFFUSION
(Selected source such as PH_3, BCl_3)

	OPERATIONAL SOLAR CELL VARIABLES																			
	I_{sc}	V_{oc}	P_{max}	η	V_{Pmax}	I_{Pmax}	FF	R_{series}	R_{shunt}	t	D	L	W	A	A_j	A_M	$(A_M/A_j) \times 100\%$	t_M	W_M	L_M
OPERATIONAL PROCESS VARIABLES																				
Furnace temperature and profile	(X)	(X)					(X)													
Time, including portions of the cycle start and finish	(X)	(X)																		
Gas mixture(s) and flow rates	(X)	(X)					(X)				(X)	(X)	(X)	(X)						
Gas purities	(X)						(X)		(X)											
Furnace tube size											X	X	X	(X)						
Furnace cleanliness	(X)	(X)					X		X											
Substrate spacing and orientation to gas flow										(X)	X	X	X	(X)	(X)					
Insertion transients	(X)																			
Removal transients	(X)																			
DIAGNOSTIC PROCESS VARIABLES																				
On a test wafer:																				
sheet resistivity	(X)	X	(X)	(X)	(X)	(X)	(X)													
junction depth	X	(X)	(X)		(X)	(X)	(X)		(X)											
oxide thickness and index of refraction																				
bulk lifetime	X	X	(X)	(X)	(X)	(X)	(X)													
surface layer lifetime	X	(X)	(X)	(X)	(X)	(X)	(X)													
Uniformity: across substrate, down furnace length		(X)					(X)													

TABLE 36B:
VARIABLES FOR DOPING BY DIFFUSION
(Selected source such as PH_3, BCl_3)

	DIAGNOSTIC SOLAR CELL VARIABLES																				
	x_j	x_m	ρ_s	ρ_{sm}	ρ_s back	X_j back	ρ	C_s	C_s back	C (x)	C (x) back	(hkl)	$N_\perp$	I_{SC} (λ)	τ	I vs V	S	R (λ)	W_B	M	Uniformi-
OPERATIONAL PROCESS VARIABLES																					
Furnace temperature and profile	(X)		(X)		(X)	(X)		X	X	X	X		(X)			(X)					(X)
Time, including portions of the cycle start and finish	(X)		(X)		(X)	(X)		X	X	X	X		(X)			(X)					(X)
Gas mixture(s) and flow rates	(X)		(X)		(X)	(X)										(X)					X
Gas purities														(X)	X	(X)	X				
Furnace tube size																					X
Furnace cleanliness													(X)	(X)	X	(X)	X				(X)
Substrate spacing and orientation to gas flow																					X
Insertion transients													(X)		(X)		(X)				(X)
Removal transients													(X)		(X)		(X)				(X)
DIAGNOSTIC PROCESS VARIABLES																					
On a test wafer:																					
sheet resistivity	(X)		*		*	(X)		(X)	(X)	(X)	(X)				(X)	(X)	(X)				
junction depth	*		(X)		(X)	*		(X)	(X)	(X)	(X)			X		(X)			(X)		
oxide thickness and index of refraction								(X)	(X)								(X)				X
bulk lifetime							X							X	*	X					
surface layer lifetime			X		X			(X)	(X)	(X)	(X)			X	X		X				
Uniformity: across substrate, down furnace length																					*

TABLE 37A:
VARIABLES FOR ION IMPLANTATION DOPING

	OPERATIONAL SOLAR CELL VARIABLES																			
	I_{sc}	V_{oc}	P_{max}	η	$V_{P_{max}}$	$I_{P_{max}}$	FF	R_{series}	R_{shunt}	t	D	L	W	A	A_j	A_M	$(A_M/A_j) \times 100\%$	t_M	W_M	L_M
OPERATIONAL PROCESS VARIABLES																				
Dopant Species	(X)	(X)					(X)													
Voltage (or Voltages)	(X)	(X)					(X)													
Analysis quality	(X)						(X)		(X)											
Beam currents and times: dose levels	(X)	(X)					(X)													
Beam power density (heating); substrate temperature																				
Substrate surface quality	(X)	(X)					(X)	(X)	(X)											
Substrate crystal orientation (channeling)	(X)	(X)					(X)		(X)											
Dielectric surface layer species and thickness	(X)	(X)																		
Surface angle	(X)	(X)																		
DIAGNOSTIC PROCESS VARIABLES																				
On a test wafer after activation annealing:																				
Sheet resistivity	(X)	X	(X)	(X)	(X)	(X)	(X)	X												
Junction depth	X	(X)	(X)	(X)	(X)	(X)	(X)		(X)											
Uniformity over a substrate		(X)					(X)													
Uniformity substrate-to-substrate																				
Bulk lifetime	X	X	(X)	(X)	(X)	(X)	(X)													
Surface layer lifetime	X	(X)	(X)	(X)	(X)	(X)	(X)	(X)												

TABLE 37A:
VARIABLES FOR ION IMPLANTATION DOPING

	DIAGNOSTIC SOLAR CELL VARIABLES																			
	x_j	x_m	ρ_s	ρ_{sm}	ρ_s back	X_j back	ρ	C_s	C_s back	$C(x)$	$C(x)$ back	(hkl)	$N_\perp$	$I_{SC}(\lambda)$	τ	I vs V	S	$R(\lambda)$	W_B	M	Uniformi
OPERATIONAL PROCESS VARIABLES																					
Dopant Species	X					X				(X)	(X)				(X)	(X)	(X)				
Voltage (or Voltages)	X					X		X	X	X	X		X	(X)			(X)				
Analysis quality															X		X				
Beam currents and times: dose levels	X		X		X	X		X	X	(X)	(X)		X	(X)		X	(X)				
Beam power density (heating); substrate temperature										(X)	(X)						(X)				(X)
Substrate surface quality	(X)					(X)		(X)	(X)												X
Substrate crystal orientation (channeling)	(X)					(X)		(X)	(X)			X									(X)
Dielectric surface layer species and thickness)	X					X		(X)	(X)												X
Surface angle	(X)					(X)		(X)	(X)												(X)
DIAGNOSTIC PROCESS VARIABLES																					
On a test wafer after activation annealing:																					
Sheet resistivity	(X)		*		*	(X)		(X)	(X)	(X)	(X)				(X)	(X)	(X)				
Junction depth	*		(X)		(X)	*		(X)	(X)	(X)	(X)			X		(X)				(X)	
Uniformity over a substrate																					*
Uniformity substrate-to-substrate																					*
Bulk lifetime							X							X	*	X					
Surface layer lifetime			X		X			(X)	(X)	(X)	(X)			X	X		X				

TABLE 38A:
VARIABLES FOR ACTIVATION ANNEALING

	OPERATIONAL SOLAR CELL VARIABLES																			
	I_{sc}	V_{oc}	P_{max}	η	$V_{P_{max}}$	$I_{P_{max}}$	FF	R_{series}	R_{shunt}	t	D	L	W	A	A_j	A_M	$(A_M/A_j) \times 100\%$	t_M	W_M	L_M
OPERATIONAL PROCESS VARIABLES																				
Temperature	(X)	(X)					(X)				X	X	X	X						
Time and heating rate	(X)	(X)									X	X	X	X						
Dose, species, and energy of implant	X	X	(X)	(X)	(X)	(X)	(X)	(X)												
Ambient gas(es) and flow rates	(X)	(X)					(X)				(X)	(X)	(X)	(X)						
Substrate spacing										(X)	X	X	X	(X)	(X)					
DIAGNOSTIC PROCESS VARIABLES																				
Sheet resistivity	(X)	X	(X)	(X)	(X)	(X)	(X)	X												
Junction depth	X	(X)	(X)	(X)	(X)	(X)	(X)		(X)											
Uniformity over a substrate		(X)					(X)													
Uniformity substrate-to-substrate																				
Bulk lifetime	X	X	(X)	(X)	(X)	(X)	(X)													
Surface lifetime	X	(X)	(X)	(X)	(X)	(X)	(X)	(X)												

TABLE 38B:
VARIABLES FOR ACTIVATION ANNEALING

	DIAGNOSTIC SOLAR CELL VARIABLES																				
	x_j	x_m	ρ_s	ρ_{sm}	ρ_s back	X_j back	ρ	C_s	C_s back	$C(x)$	$C(x)$ back	(hkl)	N_L	$I_{SC}(\lambda)$	τ	I vs V	S	$R(\lambda)$	W_B	η	Uniformity
OPERATIONAL PROCESS VARIABLES																					
Temperature	(X)		(X)		(X)	(X)		X	X	X	X		X		X	(X)	X				
Time and heating rate	(X)		(X)		(X)	(X)		X	X	X	X		X		(X)	(X)	(X)				
Dose, species, and energy of implant	X		X		X	X		X	X	(X)	(X)		X	(X)		X	(X)				
Ambient gas(es) and flow rates	(X)		(X)		(X)	(X)							(X)								X
Substrate spacing																					X
DIAGNOSTIC PROCESS VARIABLES																					
Sheet resistivity	(X)		*		*	(X)		(X)	(X)	(X)	(X)				(X)	(X)	(X)				
Junction depth	*		(X)		(X)	*		(X)	(X)	(X)	(X)			X		(X)			(X)		
Uniformity over a substrate																					*
Uniformity substrate-to-substrate																					*
Bulk lifetime							X							X	*	X					
Surface lifetime			X		X			(X)	(X)	(X)	(X)			X	X		X				

TABLE 39A:
VARIABLES FOR PLATING

	OPERATIONAL SOLAR CELL VARIABLES																			
	I_{sc}	V_{oc}	P_{max}	η	$V_{P_{max}}$	$I_{P_{max}}$	FF	R_{series}	R_{shunt}	t	D	L	W	A	A_j	A_M	$(A_M/A_j) \times 100\%$	t_M	W_M	L_M
OPERATIONAL PROCESS VARIABLES																				
Bath composition and purity of components	(X)	(X)					(X)		(X)									(X)		
Bath temperature								(X)										X		
Immersion time								(X)										X		
Agitation																		(X)		
Substrate dopant type and level																		(X)		
Bath size, life, and loading factors											X	X	X	(X)		X	(X)	X	(X)	(X)
Substrate spacing																				
Substrate surface preparation								(X)										X		
Substrate rinsing time and temperature	(X)	(X)					(X)		(X)											
Drying process	(X)																			
DIAGNOSTIC PROCESS VARIABLES																				
Metal thickness and uniformity								X										X		
Metal series resistance			(X)					X										X	X	X
Metal-silicon contact resistance			(X)					X								X			(X)	(X)
Adhesion			(X)	(X)	(X)		X	(X)	(X)							(X)		(X)	(X)	(X)
Uniformity of subsequent solder coating			(X)					X										(X)	(X)	

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TABLE 39B:
VARIABLES FOR PLATING

DIAGNOSTIC SOLAR CELL VARIABLES

	x_j	x_m	ρ_s	ρ_{sm}	ρ_s back	X_j back	ρ	C_s	C_s back	$C(x)$	$C(x)$ back	(hkl)	$N_\perp$	$I_{SC}(\lambda)$	τ	I vs V	S	$R(\lambda)$	W_B	η	Uniform
OPERATIONAL PROCESS VARIABLES																					
Bath composition and purity of components				X											X	(X)	X	(X)		X	
Bath temperature				(X)				X	X							(X)					
Immersion time				X				X	X							(X)					
Agitation				(X)				(X)	(X)												X
Substrate dopant type and level		(X)		(X)				X	X											(X)	X
Bath size, life, and loading factors																					X
Substrate spacing																					X
Substrate surface preparation		(X)		(X)				(X)	(X)						(X)	(X)	X			X	X
Substrate rinsing time and temperature															(X)	(X)	(X)	(X)			(X)
Drying process																	(X)	(X)			
DIAGNOSTIC PROCESS VARIABLES																					
Metal thickness and uniformity				X				X	X							X				X	X
Metal series resistance	(X)	(X)	X	X	X			X	X	(X)	(X)					X					
Metal-silicon contact resistance	(X)	(X)	X		X			X	X	X	X				X	X	X				
Adhesion		X													X		X			*	
Uniformity of subsequent solder coating																X				(X)	X

TABLE 40A:
VARIABLES FOR METALLIZATION SINTERING

	OPERATIONAL SOLAR CELL VARIABLES																			
	I_{sc}	V_{oc}	P_{max}	n	$V_{P_{max}}$	$I_{P_{max}}$	FF	R_{series}	R_{shunt}	t	D	L	W	A	A_j	A_M	$(A_M/A_j) \times 100\%$	t_M	W_M	L_M
<u>OPERATIONAL PROCESS VARIABLES</u>																				
Temperature	(X)	X	(X)	(X)	(X)	(X)	X	(X)	X											
Times of sequences for cycle	(X)	X	(X)	(X)	(X)	(X)	X	(X)	X											
Ambient gas and gas flow rate		(X)					(X)		(X)											
Substrate spacing											X	X	X	(X)						
<u>DIAGNOSTIC PROCESS VARIABLES</u>																				
Metal adherence																(X)		(X)		
Metal penetration into silicon	(X)	X	(X)	(X)	(X)	(X)	X		X									(X)		
Contact resistance			(X)	(X)	X		(X)	X												
Effects on photovoltaic parameters	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)											
Color changes (if silicides or oxides form)																		(X)		
Uniformity of subsequent solder coating			(X)	(X)			(X)	X										X		

TABLE 40B:
VARIABLES FOR METALLIZATION SINTERING

	DIAGNOSTIC SOLAR CELL VARIABLES																				
	x_j	x_m	ρ_s	ρ_{sm}	ρ_s back	X_j back	ρ	C_s	C_s back	$C(x)$	$C(x)$ back	(hkl)	$N_\perp$	$I_{SC}(\lambda)$	τ	I vs V	S	$R(\lambda)$	W_B	M	Uniformi
OPERATIONAL PROCESS VARIABLES																					
Temperature	(X)	X	(X)	X	(X)	(X)		(X)	(X)	(X)	(X)		(X)	(X)	X	X	X			X	(X)
Times of sequences for cycle	(X)	X	(X)	X	(X)	(X)		(X)	(X)	(X)	(X)		(X)	(X)	(X)	X	(X)			X	
Ambient gas and gas flow rate		(X)		(X)									(X)		(X)	(X)	(X)			(X)	X
Substrate spacing																				(X)	X
DIAGNOSTIC PROCESS VARIABLES																					
Metal adherence		X						(X)	(X)											*	(X)
Metal penetration into silicon		*		(X)									X		X	X	(X)			X	X
Contact resistance		X						X	X	(X)	(X)	(X)				X				X	X
Effects on photovoltaic parameters	(X)	X	(X)	X	(X)	(X)		(X)	(X)	(X)	(X)		X		X	X	(X)			X	X
Color changes (if silicides or oxides form)		X																			
Uniformity of subsequent solder coating			(X)																	(X)	X

TABLE 41A:
VARIABLES FOR SOLDER COATING

	OPERATIONAL SOLAR CELL VARIABLES																			
	I_{sc}	V_{oc}	P_{max}	η	$V_{P_{max}}$	$I_{P_{max}}$	FF	R_{series}	R_{shunt}	t	D	L	W	A	A_j	A_M	$(A_M/A_j) \times 100\%$	t_M	W_M	L_M
OPERATIONAL PROCESS VARIABLES																				
Solder composition								(X)										(X)	(X)	(X)
Flux								(X)										X	X	X
Dross inhibitor								(X)										X		
Temperature of solder							(X)		(X)									(X)		
Time in solder							(X)		(X)											
Method of substrate support										X	X	X	X	(X)				X	X	X
Contamination and bath life			(X)	(X)	(X)	(X)	(X)	X	X							X		X	X	X
Cleaning solution(s)	(X)							(X)												
DIAGNOSTIC PROCESS VARIABLES																				
Uniformity and thickness of solder coating			(X)	(X)	(X)		(X)	X										X	X	X
Series resistance of solar cell			(X)	(X)	(X)		(X)	*		(X)					(X)	X		X	X	X
Solar cell cleanliness	(X)	(X)							(X)											

TABLE 41B:
VARIABLES FOR SOLDER COATING

	DIAGNOSTIC SOLAR CELL VARIABLES																				
	x_j	x_m	ρ_s	ρ_{sm}	ρ_s back	X_j back	ρ	C_s	C_s back	$C(x)$	$C(x)$ back	(hkl)	$N_\perp$	$I_{SC}(\lambda)$	τ	I vs V	S	$R(\lambda)$	W_B	N	Uniformi-
OPERATIONAL PROCESS VARIABLES																					
Solder composition				X																X	X
Flux				(X)														(X)		X	X
Dross inhibitor				(X)														(X)		X	X
Temperature of solder		(X)													(X)		(X)			(X)	X
Time in solder		(X)													(X)		(X)			(X)	X
Method of substrate support																					X
Contamination and bath life				X																X	X
Cleaning solution(s)																		(X)			
DIAGNOSTIC PROCESS VARIABLES																					
Uniformity and thickness of solder coating		X		X												X					
Series resistance of solar cell		(X)		X												X					X
Solar cell cleanliness															(X)	(X)		(X)			(X)

after eliminating several other more direct interactions. The principal guideline for a direct relationship between a cell and process variable has been chosen to be that there is a strong, empirically observable link between changes in a process variable resulting in changes in solar cell characteristics.

For this analysis, it is assumed that the chosen process is operational. (It must be noted that, if the solar cell process were to be developed from scratch, the tables would contain many, many more relations. To do so, however, would be to ignore today's state-of-the-art.) The tables, then, form a diagnostic tool to allow observation of the effects of changing the values of the variables. It is intended that this is interactive from both the cell and the process parameters. For example, it may be utilized as a guide for trouble shooting when the cell parameters change adversely. On the other hand, it can be utilized to identify which processes and process variables should be studied for improving cell performance above some previous standard.

A further observation must be presented. Frequently, there are direct relations between operational process variables and diagnostic process variables which give only an indirect relation to some cell variables. For example, the spin-speed during a photoresist application has a direct relation to the photoresist thickness, but only an indirect relation to the linewidth of a pattern etched after exposing and developing that photoresist. Similarly, a change in a cell variable (as a result of a process variable) can result in direct effects on other cell variables, but generally will have only indirect effects on process variables.

3.6 SELECTION OF EVALUATION TECHNIQUES

The process variables have been defined as either operational or diagnostic. For purposes of selecting evaluation techniques, the diagnostic variables are, by definition, parameters which can be measured experimentally. It is clear, thus, that an experimental measurement technique will be the most suitable method for evaluating the diagnostic variables. On the other hand, categorization as an operational variable may indicate suitability for an experimental evaluation, an analytical evaluation, or both experimental and analytical evaluations.

In the process steps enumerated in previous reports, there is often redundancy of operational variables between process steps. For example, such variables as temperature, chemical purity, and substrate spacing occur in many individual process steps. For the sake of clarity and convenience, it is useful to reclassify the operational variables into categories which minimize this redundancy. This reclassification of the operational process variables, then, simplifies the definition of evaluation techniques. The categories chosen for this reclassification are listed below, along with examples for each category.

CATEGORY	EXAMPLES
1. Fundamental	Time, Temperature
2. Mechanical	Size, Spin Speed
3. Chemical	Composition, Purity
4. Logical	Diffusion Cycle, Etching Cycle
5. Energy Related	Light Intensity, RF Power

In Tables 42 - 46, the operational variables have been reclassified. Since some variables are best evaluated by direct experimental techniques, some

by analytical or theoretical techniques, and some require both experimental and theoretical analysis for optimum evaluation, the selected evaluation technique is also identified in these tables.

It is necessary to recall, when the process variables were defined, that it was assumed that the process step was itself defined, i.e., the process was running. The process variables defined are those primary variables which are necessary to specify and control, to actually allow the process to continue to perform in a satisfactory manner. This assumption, thus, recognized that a certain level of knowledge and sophistication exists in the industry today.

3.7 PERFORMANCE OF PRIMARY VARIABLE EVALUATION

Evaluation of the process variables and establishment of control ranges for these parameters is extremely process sequence dependent. Further, establishment of a process sequence is heavily dependent on the design and performance of the desired solar cell. Even having defined the exact design and structure of the cell, there are numerous choices of process sequences which can be utilized to fabricate the desired cell.

Either diffusion or ion implantation, for example, can be utilized to form a p-n junction. Each has many primary process variables which can be varied to achieve the same cell parameters. The implant must then be annealed, again giving rise to numerous process variable choices. Each could be done into either plane or textured surfaces. Each could be followed by either a plated or printed metallization. These, in turn, require dramatically different sequencing for application of the antireflection coating.

Evaluation of the performance of a process step through its many primary variables is, thus, extremely complicated and extremely dependent upon cell

TABLE 42

OPERATIONAL PROCESS VARIABLES WHICH ARE FUNDAMENTAL IN NATURE, AND SELECTED EVALUATION TECHNIQUE

VARIABLE	EVALUATION BY: ANALTYICAL	EVALUATION BY: EXPERIMENTAL
Pressure (gas, water for rinsing and scrubbing, low pressure in CVD reactor)		X
Time (dispense, bake, anneal, heat, etching, cleaning, rinsing, scrubbing, drying, exposure, development, ion implant, plating, in solder)		X
Temperature (oven, furnace, reactor, bath, gas, substrates)		X
Temperature profile (furnace, reactor, bath)		X
Volume (bath, dispense)		X

TABLE 43

OPERATIONAL PROCESS VARIABLES WHICH ARE MECHANICAL IN NATURE, AND SELECTED EVALUATION TECHNIQUE

VARIABLE	EVALUATION BY ANALYTICAL	EVALUATION BY EXPERIMENTAL
Size and Geometry (plasma chamber, furnace tube, bath)		X
Orientational and Spacing (cleaning, diffusion, CVD, plasma)		X
Substrate Support (all processes)		X
Dimensions, Tolerances, Positioning (masks, carriers, photoresist)		X
Substrate Surface (dimensions, quality, texture)		X
Substrate Crystal Orientation (oxidations, ion implant)	X	X
Substrate Preparation	X	X
Speeds (Spin, centrifuge, table)		X
Flow rates (gas, water, photoresist)		X
Flow Patterns (gas, water, photoresist)	X	X
Viscosity (photoresist, spin-ons)	X	X
Spraying Nozzle Configuration		X
Agitation (rinsing, etching)	X	X
Residues (solid, ionic, etc.)	X	X
Coverage Thickness (photoresist, metal, dielectrics)		X
Coverage Uniformity (photoresist, metal, dielectrics)		X
Adherence (photoresist, metal, dielectrics)		X

TABLE 44

OPERATIONAL PROCESS VARIABLES WHICH ARE CHEMICAL IN NATURE, AND SELECTED EVALUATION TECHNIQUE

VARIABLE	EVALUATION BY ANALYTICAL	EVALUATION BY EXPERIMENTAL
Composition (gas, chemicals, baths, I^2 shadow mask, metals, solder, flux, dross inhibitor)	X	X
Purity (chemical, gas, rinsing)	X	X
Ambient	X	X
Contamination	X	X
Residues	X	X
Ion Beam Analysis	X	X
Dielectric Layer Composition	X	X
Doping Levels (dielectrics, silicon, ion implantation, diffusion)	X	X
Dopant Species (diffusion, ion implantation)	X	X
Baths (size, life, loading factors)	X	X
Substrate Preparation (all chemical processes)		X
Etch Resistance (rate)		X
Etching End-Point Determination		X
Resist Composition		X
Spin-on Composition		X
Adherence		X

TABLE 45

OPERATIONAL PROCESS VARIABLES WHICH ARE
LOGICAL IN NATURE, AND SELECTED EVALUATION TECHNIQUE

VARIABLES	EVALUATION BY ANALYTICAL	EXPERIMENTAL
Application Sequences		X
Rinsing and Drying Cycles		X
Etching Cycles		X
CVD Sequences (Si_3N_4, Diffusion)		X
Insertion Transients (heating rates)		X
Removal Transients (cooling rates)		X
Equipment Cleaning Cycles		X

TABLE 46

OPERATIONAL PROCESS VARIABLES WHICH ARE ENERGY RELATED, AND SELECTED EVALUATION TECHNIQUE

VARIABLES	EVALUATION BY ANALYTICAL	EXPERIMENTAL
Type of Heating (RF, IR, resistance)		X
RF Power and Frequency (plasma)		X
Energy Density		X
Light Intensity (photoresist and exposure)		X
Ion Implantation:		
Voltage		X
Dose	X	X
Dose Rate	X	X

design, performance, and process sequence. It is so complicated, in fact, that it doesn't make sense to generalize a primary variable specification or evaluation. A far more logical procedure is to first specify a process sequence and cell design, empirically vary the process steps to achieve the desired result, modifying the process sequence if necessary. Only at that point does it truly make sense to perform a detailed evaluation of the process variables. Following this evaluation, the process sequence may be further modified to allow choice of optimum process control ranges.

3.8 CORRELATION AND INTERPRETATION

The correlation of process variables to cell variables, as well as to other process variables, is imperative if a high yield process is to be achieved. Both process and cell primary variables have now been defined, identifying both operational and diagnostic variables of each type. Further, first order relationships between cell and process variables have been defined.

Following the establishment of a viable process sequence, it is possible then to correlate process and cell variable interactions in a direct manner. In order for this to be useful, a feedback loop must be established between the functioning process steps in the sequence, and the evaluation of variables for both the cell and processes. The feedback must, in addition, be rapid and direct to the variable (or variables) which must be adjusted.

At this point, evaluation of the choice of process sequence and process steps must be reviewed. There must be effective ways to interpret and correlate the performance of the process variables with the cell parameters in a timely manner. There must also be no process step which

is critically dependent upon a process variable which has been evaluated to require critical control.

3.9 ESTABLISHMENT OF CONTROL RANGES

Due to the massive complexity of the interrelations of process and cell variables, the establishment of control ranges for each variable must be an iterative process. Following choice and initial verification of a process sequence, a nominal control value and range must be specified for each primary process variable. Presumably these nominal values are those which have been used to establish initial feasibility of the process sequence.

At this point each variable should be studied, one at a time, within the nominal range specified. Evaluation of the interactive effects with other process and cell variables can be determined. If process and cell parameters improve toward either end of the chosen range, the range should either be shifted or broadened. The best performance should place the optimum control value of a variable near the most cost effective region of that variable's control range. This may be at the center of the range, or perhaps skewed from the center.

Sufficient iterations through the process sequence must be performed to establish that each of the variables is optimum within the control range for that variable. This is not, however, adequate to ensure process control. A method of monitoring each variable is necessary. This monitoring may be continuous or by routine spot-checking, dependent upon the variable and the criticality of its control. Monitoring and controlling will, of necessity, add to the cost of performing the process. This cost must be traded off against the cost savings resulting from such control. The most cost effective level of monitoring and controlling will occur when the cost of

narrowing the control limits and the cost savings gained by reducing the number of rejects are equivalent.

It is obvious that each variable should be maintained at or near its optimum control value. It is very important, in addition, that the variable should be monitored adequately so that corrective adjustment of the variable can be made as it approaches either of its control limits, not when it reaches the limit. In other words, there should be an optimized probability that the variable could actually reach the limit of the control range. Conversely, the control range must be sufficiently broad, when compared to the sensitivity of the monitoring technique, that there is little chance of the limit being reached; control should be easily maintained in the cost effective region of the control range.

A large number of process steps has been identified and evaluated for possible use in process sequences which can be utilized to reach the long range goals of volume and price for solar cell modules. Utilizing technology available today, we believe that adequate control can be reached for every primary variable in the identified process steps.

4.0 COST, EQUIPMENT, AND FACILITY ASSESSMENT FOR 1982

This section presents the results of a detailed cost analysis of a factory which manufactures flat plate silicon solar photovoltaic modules. The goal of this study is to evaluate the feasibility of establishing a factory which is capable of manufacturing solar cell modules to be sold profitably at $2.00 per peak watt in 1982 (or earlier). Accordingly, the major emphasis of this study is placed on the utilization of near term technology.

4.1 ANALYSIS APPROACH

There are numerous approaches which could be chosen in the cost analysis of an as-yet unbuilt factory. Motorola, in this study, has chosen the option that the factory, equipment, direct labor, and overhead structures can be optimized for the specific function of manufacturing solar cell modules and need not be patterned after any existing factory. In addition, a very strong and basic assumption is made that the factory will manufacture only one standardized product, allowing complete redundancy for all processing equipment performing the same function.

4.1.1 TECHNOLOGY READINESS

The present study assumes that the desired factory will be manufacturing at full capacity in 1982 with a chosen technology. Due to 1) factory construction, 2) equipment purchase, construction, and installation, and 3) factory start-up (including personnel training) a significant lead time is necessary to achieve full capacity operation. The emphasis of the present

study, thus, is to include primarily manufacturing technology and equipment which is available in 1977, with any exceptions being technology now under development, but which will be secure no later than the end of 1978.

The technology readiness assumption has several significant areas of impact on costs. The most important result of this assumption is that the factory will have a limited useful life, ultimately being entirely replaced by an advanced technology which is capable of producing solar cells at a greatly reduced cost. Specifically, a factory which utilizes 1977 - 78 technology may be capable of $2.00/peak watt in 1982, but will probably not be capable of $1.00/watt in 1984 or $.50/watt by 1986. Beyond fundamental technology constrictions, other impacts are seen. Utilization of near term technology (and limited factory life) implies only moderate automation. This, in turn, leads to higher labor costs than would be seen with more complete automation.

A further impact of 1977 - 1978 technology is related to module reliability considerations. With the goal of a minimum 20 year useful life, present technology dictates stringent encapsulation requirements to protect the solar cells, leading to appreciable encapsulation costs. While this may not change significantly with advanced technology developments, the possibility exists that solar cell structures more reliable under harsh environments, or more effective cheap encapsulants, will evolve to result in lower costs.

In addition to identifying costs for 1982 manufacturing, a near term technology study provides an additional very important result: identification of areas in which technology advancement will be most fruitful for cost reduction in the next generation production plant. Technologies which have little or no possibility of meeting 1986 (and beyond) goals may be eliminated from further consideration.

4.1.2 MARKET AND FACTORY SIZE

This analysis first assumes that the factory under study will manufacture 25 megawatts in 1982 and that the entire factory is dedicated to a single product. This assumption, in turn, assumes that the market size is a minimum of 25 megawatts and that everything manufactured can be sold. The factory size assumption is made in order to assure that economies of scale, which optimize both equipment and labor, are utilized. (This assumption is later refined to allow variations in factory size in order to identify the cost dependence on factory size.)

A total market size in 1982 of 25 megawatts is a major increase over today's market. At $2.00/watt, this market size means total sales of $50 million. While this is large compared to current solar photovoltaic module sales, it is a small portion of today's total semiconductor market. The technologies utilized in solar cell manufacturing are closely related to those employed in the semiconductor industry. The technology driving force for the 1982 time frame, thus, is primarily the semiconductor industry. For later times, both larger markets and present (and future) government funded programs will contribute to larger technology advances for solar cell modules independent of the semiconductor industry.

4.2 SCOPE OF PRESENT STUDY

The present study is to determine whether or not $2.00/peak watt is a reasonable goal for 1982 (or earlier). Included in this study are identification of specific equipment, proposed factory layouts, and specific process sequences.

Motorola, during this study, has performed multiple cost analyses from which broader conclusions may be drawn. First, three different process sequences have been analyzed, two processes utilizing today's technology and a third with an advanced, longer range technology yet to be completely developed. Today's technology process sequences are a diffusion based sequence and an ion implantation sequence incorporating machines presently available. The advanced process sequence looks at the effects of a much higher beam current ion implanter than is available today.

The cost analysis in each process sequence includes all steps following polycrystalline silicon formation. This analysis includes, thus, single crystal growth, crystal slicing, wafer preparation, cell processing, cell testing, module assembly and module testing. For the process sequences investigated in this study, effects of cell size are evaluated for the entire sequence. The individual process sequences studied involve variations in only the cell processing portion of an overall sequence, leaving both the substrate formation and encapsulation portions unchanged. The two basic cell processing sequences are listed in Tables 47 and 48. These process sequences have been discussed extensively in previous reports.

Three separate solar cell size options have been evaluated. Constraints imposed on these size options are that a single solar cell module, including borders, must fit within a 120 cm (~45") square and that the module must contain an integral number of series strings of solar cells having a minimum of 33 cells per string (to guarantee a 12V battery charging capability under worst case conditions). Each cell is assumed to have an encapsulated efficiency of 14%, representing a 15% bare cell efficiency. This value is also treated as a variable, ranging from 5% to 20%, to measure cost sensitivity to this factor. The actual cell and module dimensions chosen are:

TABLE 47

SOLAR CELL DIFFUSION PROCESS SEQUENCE OUTLINE

1. Blanket P+ Diffusion, Oxide Growth
2. Front Strip and Texture Etch
3. N+ Diffusion
4. Mesa Etch
5. AR Coat
6. Front Pattern, Back Strip
7. Metal

TABLE 48

SOLAR CELL ION IMPLANTATION PROCESS SEQUENCE OUTLINE

1. Back Resist, Texture Etch
2. AR Coat
3. Front Pattern, Back Strip
4. Back I^2 - P+
5. Front I^2 (Masked) - N+
6. Activation Anneal
7. Metal

CELL DIAMETER	MODULE
7.6 cm	118 cm x 116 cm
12 cm	119 cm x 120 cm
12 cm, halved	110 cm x 113 cm

All of these sizes have been evaluated for each of the three process sequences.

Cost analyses are performed from single crystal growth through encapsulation. As a result of the 1977 - 1978 technology restriction, ingot crystal growth is assumed -- in particular, Czochralski crystal growth. This report first incorporates, as defined, a polycrystalline silicon cost of $25.00/Kg, but varies this cost later in the study to observe total sensitivity to the cost of polycrystalline silicon.

Other parameters which affect costs have been varied in this analysis to identify their cost sensitivities. In addition to the annual production volume of the factory and the cost of polycrystalline silicon, interest rate, electrical power rate, production life of the factory, and the encapsulated solar cell efficiency have each been treated as variables to determine their influence on costs.

As stated earlier, no factory now exists which can be identified with this analysis. In order to achieve such a factory, it must be built, equipped, and staffed before full production capacity can be achieved. Accordingly, this analysis incorporates these start-up costs and treats each of the sequential phases as a cost item of variable duration.

4.3 ASSUMPTIONS

It is necessary to fix certain cost inputs and assumptions in order to perform a cost analysis. These input assumptions must be carefully scrutinized when comparing separate cost analysis studies or when making

absolute judgements concerning the validity of a particular cost analysis. This section presents the assumptions and cost inputs utilized in this analysis.

4.3.1 DEFINITION OF COST CATEGORIES

In order to account for all of the costs associated with the factory, individual cost items are allocated to specific cost categories. Separate assumptions are made for each individual cost category, allowing ready examination of the costing basis of any item. The cost categories are listed and discussed in the following paragraphs. Specific assumptions for each category are then detailed in subsequent sections.

4.3.1.1 MATERIAL ITEMS

Items which appear in the final product and can be readily identified.

4.3.1.2 EXPENSE ITEMS

Items which are expended in the manufacture of product but do not appear in that product. Additional expense items not directly related to the manufacturing processes have been included in the Overhead category.

4.3.1.3 LABOR

Direct labor personnel salaries including burden and fringe benefits.

4.3.1.4 OVERHEAD ITEMS

This category contains all indirect labor, including such items as management, data processing, cafeteria, legal, training, etc. In addition, building services, indirect expense items, and all maintenance functions are included in this cost category.

4.3.1.5 INTEREST

Interest paid on all borrowed money.

4.3.1.6 DEPRECIATION

Depreciation on both buildings and capital equipment. Capital equipment is separated into that used directly for manufacturing, and that used for support functions.

4.3.2 CREATION AND LIFE OF THE FACTORY

This cost analysis assumes that the desired factory does not currently exist and must be started from the drawing-board. Four distinct phases of factory life have been identified: the building phase, equipment phase, labor training and build-up phase, and production phase.

4.3.2.1 PHASE I: BUILDING PHASE

In the building phase, a minimum staff is required to supervise the design and construction of the facility. These personnel and their several expenses are included in the first phase overhead section. Operating capital must be borrowed to pay these overhead expenses, construct the factory, and pay interest on this money during the first phase. Equipment is identified and ordered during this phase but no equipment capital is expended.

4.3.2.2 PHASE II: EQUIPMENT PHASE

In the equipment phase, all capital equipment is purchased and installed. The debt incurred in Phase I is carried into this phase. Additionally, that debt must be increased to include capital equipment expenditures as well as Phase II expense, overhead, and interest costs.

4.3.2.3 PHASE III: LABOR PHASE

During this period, the labor force is built-up and trained such that, at its conclusion, the factory is capable of running at full capacity. As in Phase II, all debts previously incurred must be included in this, the Labor Phase. Phase III material, expense, labor, overhead, and interest costs must be added to the overall debt. Although some revenue is realized from product manufactured in this phase, it is assumed that it will occur at the end of the phase and not significantly effect the magnitude of the debt.

4.3.2.4 PHASE IV: PRODUCTION PHASE

The factory is defined as running at full manufacturing capacity during this phase. At the end of this phase, there is no tapering down of the operation -- production is assumed to cease abruptly.

During this phase, income from the sale of product will be realized. It is assumed that the sum of all debts incurred in the first three phases and the debt incurred in this phase will be paid on a straight line basis over the duration of Phase IV. As a result, for the purposes of calculating interest, it is assumed that on the average half the total debt is owed over the entire duration of this phase.

4.3.2.5 FACTORY LIFE SUMMARY

The cost and income categories utilized during the four factory phases described in the previous sections are represented schematically in Figure 8. In the detailed cost analysis, each phase is treated separately. Further, the duration of each phase is treated as a variable, allowing sensitivity to each phase for the cost of the final solar cell modules to be studied.

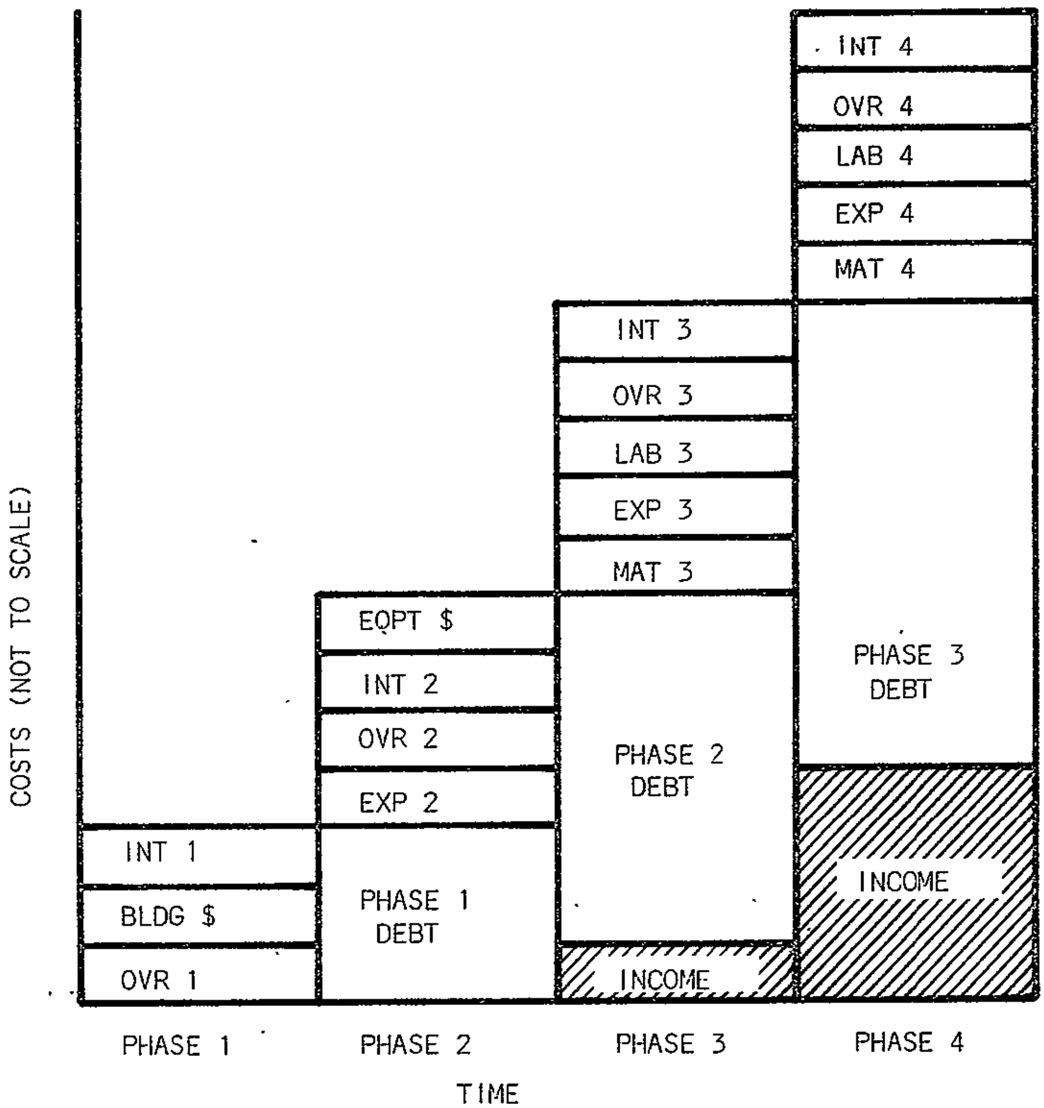

FIGURE 8 : A SCHEMATIC REPRESENTATION OF COSTS AND INCOME DURING EACH PHASE OF THE FACTORY LIFE.

4.3.3 GENERAL INPUTS AND ASSUMPTIONS

In addition to specific assumptions which can be identified with each cost category (listed in later sections) certain general assumptions and inputs must be made to form a basis for the factory. These general assumptions are listed below:

1. The factory produces only one product and supplies less than ten customers.
2. Annual production level: Treated as a variable, but 25 megawatts unless otherwise stated.
3. Solar cell efficiency: Treated as a variable, but 14% encapsulated (15% bare) unless otherwise stated.
4. Solar cell efficiency is independent of cell area.
5. Insolation assumed at 1 kilowatt/M^2 (peak).
6. Silicon wafer thickness, as sawn, is 0.008 inch.
7. Wafer diameters; 7.6 cm, 12.0 cm, and halved 12.0 cm.
8. Only one module type fabricated in the factory, chosen from three options dependent upon the cell size.
9. Total work days/year = 240, (260 - 20, vacation, holidays, etc.)

4.3.4 MATERIALS AND EXPENSE ASSUMPTIONS

The costs and sizes of specific items utilized in this analysis are listed below:

MATERIALS

Polycrystalline silicon	-	Treated as a variable, but \$25.00/Kg unless otherwise stated.

Cold Rolled Steel	-	\$0.225/lb (0.020 inch thick), \$0.204/lb (0.030 inch thick), based on 99% yield and density of 7.83 g/cm^3.
Nylon Coating	-	0.003 inch powder coating at \$0.0225/mil/ft^2.
Glass	-	3/16 inch clear tempered glass at \$10.91/4 ft. x 4 ft. sheet, 99% yield.(incoming)
Silicone	-	0.009 inch thick, \$3.75/lb (in 800 lb. drums) at 8 lbs/gallon.
Polysulfide gasket	-	\$0.60 (based on \$6/gallon).
Interconnect	-	\$0.60/ft^2, 99% yield (incoming)
Feedthroughs	-	\$0.60, (2 at \$0.30 each).

<u>D.I. WATER</u>

Volume Rate	-	\$0.0031/gal.

<u>ELECTRICITY</u>

Power rate	-	Treated as a variable, but \$0.025/kilowatt-hour unless otherwise stated.

<u>ACIDS</u>

Hydrofluoric	-	\$ 2.90/Gal.
Acetic	-	\$ 3.95/Gal.
Nitric	-	\$ 2.45/Gal.
Hydrochloric	-	\$ 2.97/Gal.

Sulfuric	-	\$ 2.45/Gal.
Buffered Hydrofluoric	-	\$ 2.95/Gal.
Waste Treatment	-	\$ 0.0020/Gal. X DIH_2O consumption

SOLVENTS

Isopropyl Alcohol	-	\$ 1.05/Gal.
Acetone	-	\$ 1.15/Gal.
Butyl Acetate	-	\$ 2.60/Gal.
VMP	-	\$ 0.75/Gal.
Photoresist (44 cps)	-	\$55.19/Gal.
Deionized Water (DIH_2O)	-	\$ 0.0031/Gal.
J100	-	\$ 7.25/Gal.

GASES

Nitrogen	-	\$ 0.0033/CF
Argon	-	\$ 0.1172/CF
Oxygen	-	\$ 0.002/CF
BCl_3	-	\$10.6061/CF
PH_3	-	\$28.0702/CF
Hydrogen	-	\$ 0.044/CF
H_2SiCl_2	-	\$ 8.6331/CF
NH_3	-	\$ 1.0619/CF

SOLUTIONS

Nickel Plating	-	\$ 0.48/liter
Palladium Plating	-	\$ 2.137/liter
Texture Etching	-	\$ 2.38/Gal.

IMPLANT SOURCES

Enriched Boron	-	\$200/lb.
Phosphorous	-	\$ 2.76/gram

4.3.5 DIRECT LABOR ASSUMPTIONS

A number of assumptions are made for direct labor, many of which are also utilized for indirect labor. As discussed in the overhead assumptions, Section 4.3.8, however, each labor category has its own salary assumption.

1. One work day = 3 shifts = 22.5 work hours; (24-1.5 lunch)
2. First shift, second shift, third shift - 8, 8, 6.5 hrs. respectively
3. Second and third shift premium = 10%
4. First shift salary rate = $4.00/hour

   (Rate with burden and fringes = $5.96/hour)
5. Absentee/turnover time loss factor = 5%
6. Miscellaneous laboratory supplies (paper towels, record forms, pencils, etc.), protective clothing, and safety equipment are assumed to be $325/year for each direct labor employee.

Examples of burden and fringe accounts are given below:

TABLE .49

BURDEN ACCOUNTS
(EXAMPLES)

1. Utility Operators
2. Employee Instruction time
3. Set-up time
4. Clean-up time
5. Coffee breaks and rest room time
6. Material handling and transfer
7. Data compilation and transfer

TABLE 50

EMPLOYEE FRINGES
(EXAMPLES)

1. Vacation
2. Holiday
3. Retirement Fund
4. Insurances
5. Cafeteria
6. F.I.C.A.
7. Unemployment Taxes
8. Credit Union
9. Employee Sales
10. Recreation Activities

4.3.6 BUILDING, DEPRECIATION, AND INTEREST ASSUMPTIONS

Assumptions utilized in determining building, depreciation, and interest costs are listed below:

1. Construction cost for production space is $80/sq. ft.
2. Construction cost for support space is $30/sq. ft.
3. Depreciation on building: Straight line for 40 years.
4. Depreciation on manufacturing equipment: Straight line over life of factory, starting after equipment is installed (at the end of Phase 2).
5. Depreciation on support equipment: Straight line for eight years.
6. Interest rate: Treated as a variable but 7% unless otherwise stated.

7. Building and support equipment sold at end of production phase to exactly offset closedown costs.

4.3.7 PROCESS STEP AND EQUIPMENT SPECIFICATIONS AND ASSUMPTIONS

This section defines the equipment specifications and assumptions for each process step utilized in all of the process sequences. Since the number of individual process steps is large, a common format is utilized for consistency. Each step is numbered for identity in the final costing data. The format utilized is as follows:

CAPITAL EQUIPMENT ASSUMPTIONS

- Type of equipment (Manufacturers model where possible)*
- Cost of equipment
- Maximum capacity of equipment (showing calculations)
- Floor space requirements (equipment and aisle and work area)
- Labor requirement

EXPENSE ITEMS

- Equipment facility requirements (electrical, exhaust, water, gases, etc.)
- Chemical and material consumption (showing calculations)
- Parts used on equipment requiring periodic replacement
- Non capitalized items necessary to perform the process (e.g., furnace tubes, beakers, etc.)

MATERIAL ITEMS

- Items appearing in finished product, (e.g., silicon, metal, module parts).

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*The specification of a given manufacturer does not necessarily mean that Motorola would prefer that manufacturer or equipment item over a competitive product. In most cases, competitive equipment exists and may be comparable or superior. Identification in this report, however, allows substantiation of information and allows direct comparison with other possible choices to determine suitability of the cost assumptions with those of other cost analysis studies.

4.3.7.1 STEP I, CRYSTAL GROWTH

Capital Equipment Assumptions

For these calculations, a Hamco CG 2000 Czochralski crystal puller costing $125K is used. The maximum capacity of this equipment is a 60 inch pull length and 20 Kg charge. Pulling rates are assumed to be 1 Kg/hour for 7.6 cm diameter crystals and 1.5 Kg/hour for 12 cm diameter crystals. Floor space is 40 ft^2. One operator can run three crystal pullers. In order to determine the usable crystal from this equipment, the following assumptions are made.

- 7.6 cm diameter cells are cut from a crystal which is grown to a diameter = 7.6 cm $\pm\,^{.6350}_{.0000}$ cm (7.9175 cm diameter average)
- 12 cm diameter cells are cut from a crystal which is grown to a diameter = 12 cm $\pm\,^{.6350}_{.0000}$ cm (12.3175 cm diameter average)
- the cropping from the tapered upper portion of the crystal will have a length of d (equal to the diameter) and an approximate volume of $\pi d^3/8$.
- the cropping from the tapered bottom portion of the crystal will have a length of d and an additional cropping from the cylindrical portion, also of length d, will result in a total cropped length of 2d and an approximate volume of $3\pi d^3/8$.
- only the portion cropped from the top of the crystal will be reclaimed.

Crystal Growth Calculations

Definition of Symbols:

ρ_{si} = Density of silicon = 2.33 g/cm^3

M = Mass of crucible charge (maximum of 20 Kg)

V_1 = Volume of cropped upper end = $\frac{\pi d^3}{8}$

V_2 = Volume of useful portion of crystal = $\frac{\pi d^2 L}{4}$

V_3 = Volume of cropped lower end = $\frac{3\pi d^3}{8}$

L = Length of useful portion of crystal

d = Diameter (average) of as-grown crystal

Calculations

$$(\rho_{si}) \left(\frac{V_1 + V_2 + V_3}{M} \right) = 1$$

$$(\rho_{si}) \left(\frac{\frac{\pi d^3}{8} + \frac{\pi d^2 L}{4} + \frac{3\pi d^3}{8}}{M} \right) = 1$$

$$L = \frac{1 - (\rho_{si}) \left(\frac{\pi d^3}{2M} \right)}{(\rho_{si}) \left(\frac{\pi d^2}{4M} \right)}$$

or

$$M = (\rho_{si})(V_1 + V_2 + V_3) = \left(\rho_{si} \right) \left(\frac{\pi d^3}{2} + \frac{\pi d^2 L}{4} \right)$$

For the 7.6 cm diameter cell,

d = 7.9175 cm (average), giving

L = 158.5 cm = 62.4 inches (for M = 20 Kg).

Since the maximum pull length of the crystal growth machine is 60 inches, this limits the actual growth of the crystal. Accordingly, the maximum actual useful crystal length is the equipment limitation minus the cropped end lengths.

L = 60 inches - 3d

L = 50.65 inches = 128.65 cm

Solving for the useful melt size,

M = 16.57 Kg

Following growth, the crystal is cropped and ground to a diameter of 7.6 cm. The resultant volume is the usable crystal for subsequent sawing. That volume has a mass of 13.6 Kg, representing 82% of the original polycrystalline silicon melt material.

For the 12 cm diameter cell,

d = 12.3175 cm (average), giving

L = 47.40 cm = 18.7 inches (for M = 20 Kg).

This length, utilizing a 20 Kg melt, is much shorter than the capacity of the crystal puller and hence is crucible limited. This will eventually lead to larger crucibles or multiple pull techniques. For this analysis, however, the conservative assumption will utilize single pulls and 20 Kg melts. Following growth, cropping and grinding, the amount of usable silicon crystal prior to sawing is 12.49 Kg, representing 62.5% of the original melt.

The crystal growth cycle is specified below:

	7.6 cm Diameter (Minutes)	12 cm Diameter (Minutes)
Charge, pump down	90	90
Melt down	120	120
Stabilize	30	30
Pull time		
neck	30	30
shoulder	60	60
straight	885 (1 Kg/hr)	526 (1.5 Kg/hr)
end	90	90
Cool down	120	120
Crystal removal - clean up	90	90
SUB TOTAL	1515	1156
X 1.05 for maintenance and repair	1591 minutes	1215 minutes
	26.5 hours	20.25 hours

Using the growth rates calculated in this section and the sawing parameters of step 4 (Section 4 .3.7.4), the crystal growth capacity is shown below in wafer equivalent form.

7.6 cm: $\frac{1 \text{ wafer}}{.0155''} \times \frac{50.65''}{\text{crystal}} \times \frac{1 \text{ crystal}}{26.50 \text{ hrs.}} = 123.25$ wafers/hour

12 cm: $\frac{1 \text{ wafer}}{.0155''} \times \frac{28.7''}{\text{crystal}} \times \frac{1 \text{ crystal}}{20.25 \text{ hrs.}} = 59.50$ wafers/hour

Expense Items

Facility requirements are:

Electrical	55 KW
Exhaust	40 CFM
Argon	35 SCFH
Chilled H_2O	30 GPM

Additional expense items include:

Crucible (12")	$47 for each crystal

4.3.7.2 STEP 2: CRYSTAL GRIND

Capital Equipment Assumptions

Grinding of the crystal to 7.6 cm or 12 cm diameter is necessary both for subsequent processing and for module unimormity. Grinding equipment costing $50K is capable of handling lengths of 40 inches/hour for 7.6 cm diameter crystals and 25 inches/hour for 12 cm diameter crystals. This equipment requires 97 ft^2 and one operator can control four grinders. The maximum length capacity for a single crystal is 23".

Expense Items

Facility Requirements

Electrical	1.5 KW
Exhaust	40 CFM

Additional expense items include:

Grinder coolant @ $3/$m^2$ of crystal surface

Silicon lost during the grinding operation is considered an expense item - in this step, it is assumed that the crystal

is grown to an average diameter of 7.9175 cm or 12.3175 cm and ground to a final diameter of 7.6 cm or 12 cm respectively. The length of the crystal is either 128.65 cm or 47.40 cm respectively. From these numbers, the volume of wasted silicon from the grinding operation can be calculated. The volume of silicon ground off is the volume of the useful as-grown crystal minus the volume of the crystal ground to size.

Definition of Terms

V_G = Volume lost during grinding

M_G = Mass of ground crystal

d_I = As-grown diameter

d_F = Final crystal diameter

L = Length of useful portion of silicon

t = Thickness of as-sawn wafer plus thickness of sawing kerf

N_G = Number of wafers/crystal

ρ_{si} = Density of silicon (2.33 g/cm^3

P_p = Price of polycrystalline silicon ($/Kg)

C_G = Cost of ground-off crystal surface material/1000 wafers

Calculations

$$V_G = \frac{\pi L}{4}\left(d_I{}^2 - d_F{}^2\right)$$

$$M_G = V_G \, \rho_{si}$$

$$N_G = \frac{L}{t}$$

$$C_G = \left(\frac{M_G}{N_G}\right)(P_p)(1000)$$

For the 7.6 cm diameter cell

$$V_G = \frac{\pi\ (128.65\ cm)\ [(7.9175cm)^2 - (7.6\ cm)^2]}{4}$$

$$V_G = 497.8\ cm^3$$

$$M_G = (497.8\ cm^3)(2.33\ g/cm^3) = 1.16\ Kg$$

$$N_G = \frac{(128.65\ cm)}{(0.0394\ cm/wafer)} = 3267\ wafers$$

$$C_G = \left(\frac{1.16\ Kg}{3267\ wafers}\right)(P_p)(1000) = \$0.355\ P_p \text{ per 1000 wafers}$$

For the 12 cm diameter cell

$$V_G = \frac{\pi(47.40\ cm)\ [(12.3175\ cm)^2 - (12.0\ cm)^2]}{4}$$

$$V_G = 287.4\ cm^3$$

$$M_G = (287.4\ cm^3)(2.33\ g/cm^3) = 0.670\ Kg$$

$$N_G = \frac{(47.4\ cm)}{(0.0394\ cm/wafer} = 1204\ wafers$$

$$C_G = \left(\frac{0.670\ Kg}{1204\ wafers}\right)(P_p)\ (1000) = \$0.556\ P_p \text{ per 1000 wafers}$$

4.3.7.3 STEP 3: CRYSTAL CROPPING

Capital Equipment Assumptions

Crystals to be sawed into wafers must first be cropped and sawed into appropriate length pieces to fit into the wafer sawing apparatus. The equipment used to perform this operation is an O.D. diamond saw costing approximately \$8000 including the necessary fixtures. Floor space is expected to be 40 ft^2. Cutting time is based on 3"/minute plus 30 seconds/cut set-up time.

Expense Items

Facility requirements include:

Electrical	=	6 KW
Exhaust	=	100 CFM

Additionally, blades must be replaced after 10,000 cuts. Assuming 14 cuts for 7.6 cm diameter crystals and 6 cuts for 12 cm diameter crystals which result in 3267 wafers and 1204 wafers respectively then 2333571 and 2006667 wafer equivalents can be expected for each $425 blade resulting in a blade expense of $0.1821 per thousand wafers for 7.6 cm diameter crystals and $0.2118 per thousand wafers for 12 cm diameter crystals.

In this step, the upper and lower portions of the crystal are removed, each having volumes of $\pi d^3/8$ and $3\pi d^3/8$ respectively, with d = 7.9175 or 12.3175 cm. If the upper portion of the crystal is reclaimed for remelt, the resultant loss of silicon from the lower end is then $3\pi d^3/8$.

Definition of Terms

V_3	=	Volume of lower cropped end
M_3	=	Mass of cropped lower crystal end
ρ_{si}	=	Density of silicon
N_G	=	Number of wafers/crystal
t	=	Thickness of as-sawn wafer plus thickness of sawing kerf
L	=	Length of useful portion of silicon crystal
d_I	=	As-grown diameter of crystal
P_p	=	Price of polycrystalline silicon ($/Kg)
C_3	=	Cost of cropped lower end of crystal/1000 wafers

Calculations

$$V_3 = \frac{3\pi \, d_I{}^3}{8}$$

$$M_3 = V_3 \rho_{si}$$

$$N_G = \frac{L}{t}$$

$$C_3 = \left(\frac{M_3}{N_G}\right)(P_p)(1000)$$

For the 7.6 cm diameter solar cell,

$$V_3 = \frac{3\pi\ (7.9175\ \text{cm})^3}{8} = 584.7\ \text{cm}^3$$

$$M_3 = (584.7\ \text{cm}^3)(2.33\ \text{g/cm}^3) = 1.362\ \text{Kg}$$

N_G = 3267 wafers (from process step #2 calculations)

$$C_3 = \left(\frac{1.362\ \text{Kg}}{3267\ \text{wafers}}\right)(P_p)(1000)$$

$$= \$0.417\ P_p \text{ per 1000 wafers}$$

For the 12 cm diameter solar cell,

$$V_3 = \frac{3\pi\ (12.3175\ \text{cm})^3}{8} = 2202\ \text{cm}^3$$

$$M_3 = (2202\ \text{cm}^3)(2.33\ \text{g/cm}^3) = 5.13\ \text{Kg}$$

N_G = 1204 wafers (from process step 2 calculations)

$$C_3 = \left(\frac{5.13\ \text{Kg}}{1204\ \text{wafers}}\right)(P_p)(1000)$$

$$= \$4.26\ P_p \text{ per 1000 wafers}$$

4.3.7.4 STEP 4: CRYSTAL SAWING

Capital Equipment Assumptions

The sawing operation will require a wire saw which costs $30K for cutting 7.6 cm diameter crystals and $35K for cutting 12 cm diameter crystals. It will need a 40 ft^2 floor space and 0.1 and 0.05 operators per saw respectively. 7.6 cm wafers will be cut at the rate of 86 wafers/hour. 12 cm wafers will be cut at the rate of 34.4 wafers/hour. As-cut wafer thickness is 9.02032 cm (8 mils).

Expense Items

Facility requirements:

Electrical	1 KW
Raw Water	1 GPM

Kerf loss for a saw cut is assumed to be 0.01905 cm (7.5 mil) for all crystal diameters). The number of cuts to produce 1000 wafers will be at least 999.

Definition of Terms

V_K = Volume of kerf/1000 wafers

N_K = Number of cuts/1000 wafers

d_F = Diameter of final crystal

P_p = Price of polycrystalline silicon ($/Kg)

ρ_{si} = Density of silicon = 2.33 g/cm^3

t_K = Thickness of kerf per cut

C_K = Cost of kerf silicon/1000 wafers

Calculations

$$V_K = \frac{N_K\ t_K \pi d_F^2}{4}$$

$$C_K = V_K\ \rho_{si}\ P_p$$

For the 7.6 cm diameter solar cell,

$$V_K = (999 \text{ cuts}) \left(\frac{0.01905 \text{ cm}}{\text{cut}}\right) \left(\frac{\pi}{4}\right) (7.6 \text{ cm})^2$$

$$V_K = 863.3 \text{ cm}^3$$

$$C_K = (863.3 \text{ cm}^3)\ (2.33 \text{ g/cm}^3)\ (1 \text{ Kg}/1000 \text{ g})\ P_p$$

$$C_K = \$2.01\ P_p \text{ per } 1000 \text{ wafers}$$

For the 12 cm diameter solar cell,

$$V_K = (999 \text{ cuts}) \left(\frac{0.01905 \text{ cm}}{\text{cut}}\right) \left(\frac{\pi}{4}\right) (12 \text{ cm})^2$$

$$V_K = 2152 \text{ cm}^3$$

$$C_K = (2152 \text{ cm}^3)\ (2.33 \text{ g/cm}^3)\ (1 \text{ Kg}/1000 \text{ g})\ P_p$$

$$C_K = \$5.01\ P_p \text{ per } 1000 \text{ wafers}$$

Additional major expense items are the cost of supplies used during the sawing operation which include slurry, wire, wire guides, and miscellaneous supplies. These expenses total \$13.79 per square meter of silicon wafers.

4.3.7.5 STEP 5: CLEAN ETCH

Capital Equipment Assumptions

This process step is intended to remove from the silicon wafers damage induced during the sawing operation. An in-line ultrasonic tank containing a caustic etch will be used. This equipment costs \$75K, requires one operator and 360 ft^2; 228 wafers can be cleaned and etched in 10 minutes resulting in a process rate of 1368 wafers/hour.

Expense Items

Facility requirements are:

Electrical	10 KW
Exhaust	600 CFM
DIH_2O	5 gpm

In this process step, 0.5 mil will be etched from both sides of each wafer resulting in a 1 mil (.00254 cm) silicon loss per wafer.

An additional expense item is the caustic etch. 15% $NaOH:H_2O$ will be used in a 22 gal. tank, changed daily and costing \$0.05/gal. = \$5000/year.

Definition of Terms

t_W = Thickness of final wafer

t_E = Thickness of silicon etched from sawed wafer

d_F = Final diameter of wafer

ρ_{si} = Density of silicon

V_E = Volume of etched silicon/1000 wafers

P_p = Price of polycrystalline silicon (\$/Kg)

C_E = Cost of etched-away silicon/1000 wafers

V_W = Volume of wafers after etching/1000 wafers

C_W = Cost of silicon in final wafers/1000 wafers

Calculations

$$V_E = (t_E)\left(\frac{\pi d_F^2}{4}\right)(1000)$$

$$C_E = V_E \, \rho_{si} \, P_p$$

$$V_W = (t_W)\left(\frac{\pi d_F^2}{4}\right)(1000)$$

$$C_W = V_W \, \rho_{si} \, P_p$$

For the 7.6 cm diameter solar cell,

$$V_E = (2.54 \text{ cm}) \left(\frac{\pi}{4}\right) (7.6 \text{ cm})^2$$

$$V_E = 115.23 \text{ cm}^3$$

$$C_E = (115.23 \text{ cm}^3)(2.33 \text{ g/cm}^3) \, P_p \, (1 \text{ Kg}/1000 \text{ g})$$

$$C_E = \$0.268 \, P_p \text{ per 1000 wafers}$$

For the 12 cm diameter solar cell,

$$V_E = (2.54 \text{ cm}) \left(\frac{\pi}{4}\right) (12 \text{ cm})^2$$

$$V_E = 287.3 \text{ cm}^3$$

$$C_E = (287.3 \text{ cm}^3)(2.33 \text{ g/cm}^3) \, P_p \, (1 \text{ Kg}/1000 \text{ g})$$

$$C_E = \$0.669 \, P_p \text{ per 1000 wafers}$$

Material Items

Silicon wafers are treated in this step, for the first and only time, as a material item. Wafer thickness is assumed to be 7 mil (0.0178 cm).

For the 7.6 cm diameter wafer,

$$V_W = (17.8 \text{ cm}) \left(\frac{\pi}{4}\right) (7.6 \text{ cm})^2$$

$$V_W = 807.5\ cm^3$$

$$C_W = (807.5\ cm^3)(2.33\ g/cm^3)\ P_p\ (1\ Kg/1000\ g)$$

$$C_W = \$1.88\ P_p \text{ per 1000 wafers}$$

For the 12 cm diameter wafer,

$$V_W = (17.8\ cm)\ (\tfrac{\pi}{4})(12\ cm)^2$$

$$V_W = 2013\ cm^3$$

$$C_W = (2013\ cm^3)(2.33\ g/cm^3)\ P_p\ (1\ Kg/1000\ g)$$

$$C_W = \$4.69\ P_p \text{ per 1000 wafers}$$

4.3.7.6 STEP 6: CENTRIFUGE

Capital Equipment Assumptions

Cost estimates are based on the use of a Fluoroware K-100 rinser-dryer with a #1150 frame and a #1231 cradle, all of which are intended to process 7.6 cm diameter wafers. This apparatus will hold six 25 wafer cassettes and costs $2500. Use of a different cradle will allow the processing of four 25 wafer (12 cm diameter) cassettes for the same price. For both wafer diameters, a 15 minute cycle time (including load and unload) will be assumed, resulting in a throughput of:

For 7.6 cm diameter wafers,

$$\frac{25 \text{ wafers}}{\text{cassette}} \times \frac{6 \text{ cassettes}}{\text{machine}} \times \frac{4 \text{ runs}}{\text{hour}} = \frac{600 \text{ wafers}}{\text{machine-hour}}$$

For 12 cm diameter wafers,

$$\frac{25 \text{ wafers}}{\text{cassette}} \times \frac{4 \text{ cassettes}}{\text{machine}} \times \frac{4 \text{ runs}}{\text{hour}} = \frac{400 \text{ wafers}}{\text{machine-hour}}$$

Floor space required for this equipment is estimated to be 30 ft^2. One operator will run four units.

Expense Items

Facility requirements include:

Electrical	1 KW (115 VAC - 8.5 A)
DIH_2O	1.6 GPM @ 40 psi
N_2	13.2 ℓ/min @ 40 psi

Assume two wafer carriers for each slot in the cradle, one in use and one being loaded or unloaded.

7.6 cm: 12 carriers x \$19.20/carrier = \$230.40/machine

12 cm: 8 carriers x \$32.00/carrier = \$256.00/machine

4.3.7.7 STEP 7: TEXTURE ETCH

Capital Equipment Assumptions

Equipment used in the texture etch process includes a six foot laminar flow exhaust hood (IAS LV6 - 30X) containing six etch tanks (7" wide x 6" deep x 20" long) and a chemical recirculating system (Fluorocarbon Model 5000) which is used to maintain the etch integrity. The cost of the hood is \$4500 and the recirculating system costs \$7500 resulting in a total system cost of \$12K. Assuming a one hour process time:

$$\text{7.6 cm cell:} \quad \frac{\text{50 wafers}}{\text{carrier}} \times \frac{\text{4 carriers}}{\text{sink}} \times \frac{\text{6 sinks}}{\text{hood}} = \frac{\text{1200 wafers}}{\text{hour}}$$

$$\text{12 cm cell:} \quad \frac{\text{50 wafers}}{\text{carrier}} \times \frac{\text{3 carriers}}{\text{sink}} \times \frac{\text{6 sinks}}{\text{hood}} = \frac{\text{900 wafers}}{\text{hour}}$$

Floor space is 45 ft^2 and one operator is necessary for two such hoods.

Expense Items

Facility requirements include:

Electrical	1.6 KW
Exhaust	500 CFM

Assumptions used in the cost analysis for chemicals are as follows:

7.6 cm: Displacement of carrier and 50 wafers is 300 cm^3.

Assuming a liquid level of 4" when four loaded carriers are placed in the tank, then:

$$\left(\frac{9177\ cm^3}{tank} - \frac{300\ cm^3}{carrier}\right) X \left(\frac{4\ carriers}{tank}\right) X \frac{6\ tanks}{hood} X \frac{2.64 \times 10^{-4}\ gal}{cm^3} = \frac{12.6356\ gal}{hood}$$

Utilizing a recirculating system to maintain etch solution integrity, it is assumed that, on the average, the entire solution will be replaced every four days, which results in 60 annual chemical replacements. Therefore:

$$\frac{12.6356\ gal}{hood} X \frac{\$2.38}{gal.} X \frac{60}{year} = \frac{\$1803}{year}\ \text{(chemical cost) per hood}$$

= \$0.28/1000 wafersif the equipment is fully utilized.

12 cm: Displacement of carrier and 50 wafers is 515 cm^3.

Assuming a liquid level of 6" when three loaded carriers are placed in the tank, then:

$$\left(\frac{13765\ cm^3}{tank} - \frac{515\ cm^3}{carrier}\right) X \left(\frac{3\ carriers}{tank}\right) X \frac{6\ tanks}{hood} X \frac{2.64 \times 10^{-4}\ gal}{cm^3} = \frac{19.3567\ gal.}{hood}$$

Using the same assumptions as for 7.6 cm wafers,

$$\frac{19.3567\ gal}{hood} X \frac{\$2.38}{gal.} X \frac{60}{year} = \frac{\$2762}{year}\ \text{(chemical costs) per hood}$$

$= \frac{\$0.57}{1000\ wafers}$ if the equipment is fully utilized.

Additional expense items include:

Carriers:

7.6 cm: $2 \times \frac{4 \text{ carriers}}{\text{sink}} \times \frac{6 \text{ sink}}{\text{hood}} \times \frac{\$19.20}{\text{carrier}} = \$921.60\text{/year per hood}$

= $0.14/1000 wafers if fully utilized.

12 cm: $2 \times \frac{3 \text{ carriers}}{\text{sink}} \times \frac{6 \text{ sink}}{\text{hood}} \times \frac{\$32.00}{\text{carrier}} = \$1152.00\text{/year per hood}$

= $0.24/1000 wafers if fully utilized.

Quartzware: Assume $\$1/in^2$ for quartz liners which results in

$$\frac{464 \text{ in}^2}{\text{liner}} \times \frac{6 \text{ liners}}{\text{hood}} \times \frac{\$1}{\text{in}^2} = \$2784\text{/hood}$$

These liners should have a two year life resulting in $1392/year cost. The liner cost is thus $0.21/1000 wafers (7.6 cm) and $0.27/1000 wafers (12 cm) assuming 100% equipment utilization.

4.3.7.8 STEP 8: COAT, BAKE, AND STEP 11: ETCH STOP APPLY

Capital Equipment Assumptions

Equipment specified for this process is a Macronetics coater-oven unit capable of containing four separate tracks, each costing $13,365. Additional costs for this unit are a cabinet costing $3,000 and a hood (IAS LV10-30) costing $2,500. Assuming a complete, four track unit, total capital cost of $58,960. Each track is capable of processing 250 wafers/hour and a unit will require 80 ft^2. One operator can control two four track systems.

Expense Items

Facility requirements are:

Electrical	1.1 KW + 2.5 KW/track
Exhaust	120 CFM/track

Additional expense items include the cost of photoresist. For this analysis, it is assumed that an excess of resist is used while coating and that both 7.6 cm and 12 cm diameter wafers can be coated at 9470 wafers/gallon. Cost of the photoresist is $55.19/gallon resulting in an expense of $5.83/1000 wafers.

All assumptions apply to both process steps (8 and 11).

4.3.7.9 STEP 9: ALIGN, EXPOSE

Capital Equipment Assumptions

A Kasper 2001P aligner with automatic loading, costing $30,000, has been specified for this operation. A hood costing $1250 will be used for this equipment, and total capacity is assumed to be 200 wafers/hour. Floor space is 40 ft^2 and one operator is required for each aligner.

Expense Items

Facility requirements are:

Electrical	1.5 KW

Exposure lamps which have an average life of 1500 operating hours and cost $42 add $151.20/year to the operating expenses - $0.14/1000 wafers.

4.3.7.10 STEP 10: DEVELOP, BAKE

Capital Equipment Assumptions

This process step utilizes a Macronetics developer-oven unit capable of containing four separate tracks, each costing $13,100. Additional costs for this unit are a cabinet costing $3,000 and a hood (IAS LV10-30) costing $2,500. Assuming a complete, four track unit, total capital cost if $57,900.

Each track is capable of processing 250 wafers/hour and a unit will require 80 ft^2. One operator can control eight individual tracks (or two systems).

Expense Items

Facility requirements are:

Electrical	1.1 KW + 2.5 KW/track
Exhaust	120 CFM/track

Additional expense items include the cost of developer at $1.675/gallon. This developer can process 240 wafers (7.6 cm or 12 cm diameter) resulting in a $6.98/1000 wafer expense.

4.3.7.11 STEP 12: BORON DIFFUSION

Capital Equipment Assumptions

This process step assumes a Thermco eight-tube diffusion module, Type 4000S72 per Spec 19000 with load station, source cabinets and appropriate options at $49,271. Process controllers are estimated to be $2,000/tube, resulting in a total system cost of $65,271.

One operator will run the system, assuming a one hour average process time. Using 25 wafer dump transfer type boats, 125 wafers/tube or 1000 wafers/hour can be processed. Floor space required for this diffusion system is 275 ft^2.

Expense Items

Facility requirements are:

Electrical	140 KW
Exhaust	125 CFM

Doping and carrier gases:

BCl_3 @ $\frac{0.4138 \text{ cc}}{\text{wafer}} \times \frac{\$0.3745}{1000 \text{ cc}} = \$0.1546/1000$ wafers

N_2 @ $\frac{3 \text{ ft}^3}{\text{hour}} \times \frac{\$0.0033}{\text{ft}^3} \times \frac{1 \text{ hour}}{\text{run}} \times \frac{1 \text{ run}}{125 \text{ wafers}} = \$0.0792/1000$ wafers

Quartzware: (assumes tubes and boats replaced annually) = \$769/year per tube = \$1.14/1000 wafers, assuming 100% utilization of the equipment.

4.3.7.12 STEP 13: PHOSPHORUS DIFFUSION

Capital Equipment Assumptions

This process step assumes a Thermco eight-tube diffusion module, Type 4000S72 per Spec 19000 with load station, source cabinets and appropriate options at \$49,271. Process controllers are estimated to be \$2,000/tube, resulting in a total system cost of \$65,271.

One operator will run the system assuming a one hour average process time. Using the 25 wafer dump transfer type boat, 125 wafers/tube or 1000 wafers/hour can be processed. Floor space required for this diffusion system is 275 ft^2.

Expense Items

Facility requirements are:

Electrical	140 KW
Exhaust	125 CFM

Doping and carrier gases:

PH_3 @ $\frac{0.1164 \text{ ft}^3}{1000 \text{ wafers}} \times \frac{\$28.07}{\text{ft}^3} = \frac{\$3.27}{1000 \text{ wafers}}$

Argon @ $\frac{14.8 \text{ ft}^3}{1000 \text{ wafers}} \times \frac{\$0.1172}{\text{ft}^3} = \frac{\$1.73}{1000 \text{ wafers}}$

Quartzware: (assume tubes and boats replaced annually = \$769/year per tube

= \$1.14/1000 wafers,

assuming 100% utilization of the equipment.

4.3.7.13 STEP 14: DRIVE-IN DIFFUSION

Capital Equipment Assumptions

This process step assumes a Thermco eight-tube diffusion module Type 4000S72 per Spec 19000 with load station, source cabinets and appropriate options at \$49,271. Process controllers are estimated to be \$2,000/tube resulting in a total system cost of \$64,271.

One operator will run the system, assuming a one hour average process time. Using the close pack (50 wafer) dump transfer type boat, 250 wafers/tube or 2000 wafers/hour can be processed. Floor space required for this diffusion system is 275 ft^2.

Expense Items

Facility requirements are:

Electrical	140 KW per module
Exhaust	125 CFM per module
N_2	3 ℓ/min. per tube

$$\frac{3\,\ell}{\text{min.}} \times \frac{60\text{ min.}}{\text{Hr.}} \times \frac{.0353\text{ CF}}{\ell} \times \frac{5400\text{ hr.}}{\text{year}} \times \frac{\$.0033}{\text{CF}} = \$113.25/\text{year per tube}$$

Quartzware: (assume tubes and boats replaced annually = \$769/year per tube.

N_2 and Quartzware, thus, represent \$0.084 and \$0.57, respectively, per 1000 wafers assuming 100% utilization of the equipment.

4.3.7.14 STEPS 15 AND 38: ION IMPLANTATION

Capital Equipment Assumptions

Today's available implantation technology has been used to estimate the cost of an ion implantation process. The equipment specified is an Extrion 200-1000 implanter which costs approximately \$300,000. Maximum throughput for 7.6 cm diameter wafers is 80/hour. By modifying the wafer holder, it is anticipated that 12 cm diameter wafers can be processed at the rate of 40/hour. Floor space requirement is 400 ft^2 and one operator can control 2 implanters.

Expense Items

Facility requirements include:

Electrical	20 KW
Exhaust	200 CFM
DIH_2O	5 GPM

Additional expense items are:

$$LN_2: \frac{5\ \ell}{\text{shift}} \times \frac{3\ \text{shift}}{\text{day}} \times \frac{240\ \text{day}}{\text{year}} \times \frac{28.32\ \text{CF}}{\ell} \times \frac{\$.0026}{\text{CF}} = \frac{\$265}{\text{year}}$$

Assuming 100% utilization of the equipment, the cost of LN_2 is:

7.6 cm: \$0.61/1000 wafers

12 cm: \$1.22/1000 wafers

Wafer holders are assumed to be included in the original capital cost.

For phosphorus implants,

$$\frac{6.0225 \times 10^{23}\ \text{atoms}}{30.9738\ \text{g (Phos)}} = \frac{1.944 \times 10^{22}\ \text{atoms}}{\text{gram}}$$

At 10% efficiency, available source = 1.944×10^{21} atoms/gram.

Selecting an implant of 2×10^{15} atoms/cm^2, then:

7.6 cm diameter cells

$$\frac{2 \text{ X } 10^{15} \text{ atoms}}{\text{cm}^2} \text{ X } \frac{45.36 \text{ cm}^2}{\text{wafer}} \text{ X } \frac{\$2.76}{\text{gram}} \text{ X } \frac{1 \text{ gram}}{1.944 \times 10^{21} \text{ atoms}} = \frac{\$0.1288}{1000 \text{ wafers}}$$

12 cm diameter cells

$$\frac{2 \text{ X } 10^{15} \text{ atoms}}{\text{cm}^2} \text{ X } \frac{113.097 \text{ cm}^2}{\text{wafer}} \text{ X } \frac{\$2.76}{\text{gram}} \text{ X } \frac{1 \text{ gram}}{1.944 \text{ X } 10^{21} \text{ atoms}} = \frac{\$0.3211}{1000 \text{ wafers}}$$

For boron implants,

$$\frac{6.0225 \times 10^{23} \text{ atoms}}{10.811 \text{ g (Boron)}} = 5.5707 \text{ X } 10^{22} \text{ atoms/gram}$$

At 2% efficiency, available source = $1.1141 \text{ X } 10^{21}$ atoms/gram

Selecting an implant of $1 \text{ X } 10^{15}$ atoms/cm^2, then:

7.6 cm diameter cells

$$\frac{1 \text{ X } 10^{15} \text{ atoms}}{\text{cm}^2} \text{ X } \frac{45.36 \text{ cm}^2}{\text{wafer}} \text{ X } \frac{\$0.4409}{\text{gram}} \text{ X } \frac{1 \text{ gram}}{1.1141 \text{ X } 10^{21} \text{ atoms}} = \frac{\$0.018}{1000 \text{ wafers}}$$

12 cm diameter cells

$$\frac{1 \text{ X } 10^{15} \text{ atoms}}{\text{cm}^2} \text{ X } \frac{113.097 \text{ cm}^2}{\text{wafer}} \text{ X } \frac{\$0.4409}{\text{gram}} \text{ X } \frac{1 \text{ gram}}{1.1141 \text{ X } 10^{21} \text{ atoms}} = \frac{\$0.0448}{1000 \text{ wafers}}$$

Vacuum pump oil is expected to be changed on a bi-monthly basis.

At $17.42/bottle, total annual cost is expected to be $418.

Pump oil is:

7.6 cm: $0.97/1000 wafers

12 cm: $1.94/1000 wafers

4.3.7.15 STEPS 16 AND 37: ADVANCED ION IMPLANTATION

This system will use an unanalyzed ion beam system. Current cost and capacity estimates anticipate that a 100 mA phosphorus system and a 10 mA boron system can be purchased for $85K. Utilizing a belt transport system through a differentially pumped vacuum chamber, implant times will probably

be mechanically limited to 0.5 sec/wafer. The chart below shows estimated implant times and throughputs.

	7.6 cm Cell		
	Calculated time (sec)	Machine time (sec)	Throughput (WPH)
Phosphorous (2×10^{15} @ 100 mA)	.2686	.5	7200
Boron (1×10^{15} @ 10 mA)	1.3429	1.5	2400
Boron (8×10^{14} @ 10 mA)	1.0743	1.25	2889

	12 cm Cell		
	Calculated time (sec)	Machine time (sec)	Throughput (WPH)
Phosphorous (2×10^{15} @ 100 mA)	.6696	.75	4800
Boron (1×10^{15} @ 10 mA)	3.348	3.5	1030
Boron (8×10^{14} @ 10 mA)	2.6784	2.75	1310

Floor space is assumed to be 400 ft^2 and one operator is required for each implanter.

Expense Items

Electrical	50 KW
Exhaust	40 CFM
DIH_2O	10 GPM

Expense items for LN_2, vacuum pump oil, and ion sources listed in Section 4.3.7.14.

4.3.7.16 STEP 17: SILICON NITRIDE

Capital Equipment Assumptions

This process step assumes a Thermco eight-tube diffusion module, Type 4000S72 per Spec 19000 with load station, source cabinets and appropriate

options at \$49,271. Process controllers estimated to be \$2,000/tube result in a total system cost of \$65,271.

One operator will run the system, assuming a one hour average process time. Using the close pack (50 wafer) dump transfer type boat, 250 wafers/tube, or 2000 wafers/hour, can be processed. Floor space required for this system is 275 ft^2.

Expense Items

Facility requirements are:

Electrical	140 KW
Exhaust	125 CFM

Gases used in the formation of this dielectric anti-reflection layer are shown below:

$$H_2SiCl_2: \quad \frac{10\ cm^3}{min} \times \frac{60\ min}{hr} \times \frac{5400\ hr}{year} \times \frac{3.53 \times 10^{-5}\ CF}{cm^3} \times \frac{\$8.6331}{CF} = \frac{\$987.50}{year}$$

$$NH_3: \quad \frac{15\ cm^3}{min} \times \frac{60\ min}{hr} \times \frac{5400\ hr}{year} \times \frac{3.53 \times 10^{-5}\ CF}{cm^3} \times \frac{\$1.0619}{CF} = \frac{\$181.25}{year}$$

Assuming that this equipment is 100% utilized, H_2SiCl_2 and NH_3 represent costs of \$0.73/1000 wafers and \$0.13/1000 wafers, respectively.

Quartzware: (assume tubes and boats replaced annually) = \$769/year per tube = \$0.57/1000 wafers, assuming 100% utilization of the equipment.

4.3.7.17 STEP 18: HIGH PRESSURE SCRUBBER

Capital Equipment Assumptions

This process step uses a Macronetics HPC-1000. To normalize floor space, a four track unit is suggested. Cost items are as follows:

Scrubber @ \$12,925/track	=	\$51,700
Four track cabinet	=	3,000
Laminar flow hood	=	1,795
TOTAL		\$56,495

It is anticipated that a four track unit can process 1000 wafers/hour and will require one operator. Floor space is estimated to be 45 ft^2.

Expense Items

Electrical	1.1 KW + 0.25 KW/track
Exhaust	80 CFM/track
DIH_2O	0.8 GPM/track

4.3.7.18 STEP 19: PLASMA CLEAN

Capital Equipment Assumptions

It is anticipated that a two chamber unit, each capable of containing two 50 wafer carriers, will be used. A complete cycle will be 15 minutes including pump down, ash, and vent. Since only one chamber can be operated with rf power at a time, the other will be vented, unloaded, loaded, and pumped down and waiting for the 10 minute ashing cycle. Thus, six runs/hour X 100 wafers/run result in a throughput of 600 wafers/hour. It is expected that a plasma asher of this type can be bought for \$15K. Floor space is 30 ft^2 and one operator can run two units.

Expense Items

Electrical	1.5 KW
Exhaust	40 CFM

Vacuum pump oil @ $\frac{\$17.42}{\text{bottle}} \times \frac{24 \text{ bottles}}{\text{year}} = \frac{\$418.08}{\text{year}} = \frac{\$0.13}{1000 \text{ wafers}}$,

assuming 100% utilization of the equipment.

4.3.7.19 STEPS 20, 21, 22: MESA ETCH 1 and 2, RINSE, DRY

Capital Equipment Assumptions

The sequence used for these process operations is:

1. 30 sec silicon etch in a 5:1:4 HNO_3:Acetic:HF mixture
2. 5 min DIH_2O rinse
3. 3 min rinse-dry
4. 15 min plasma clean
5. 15 sec in a 4:1 NH_4:HF solution
6. 5 min DIH_2O rinse

Operations 1 and 2 will be performed in a six foot laminar flow exhaust hood (IAS LV6-30X) containing six etch tanks (7 inches wide X 6 inches deep X 20 inches long) and a wafer carrier transport system. Three of the tanks will contain the etch solution and three will be utilized for the DIH_2O rinse operation. Each wafer carrier will contain 50 wafers. Cost of this hood is \$4.5K. Floor space is 45 ft^2 and one operator is required. These two operations will require 6 minutes (10/hr) and result in the following hood capacity:

$$\text{7.6 cm cell:} \quad \frac{200 \text{ wafers}}{\text{tank}} \times \frac{3 \text{ sinks}}{\text{hood}} \times \frac{10 \text{ runs}}{\text{hour}} = \frac{6000 \text{ wafers}}{\text{hour}}$$

$$\text{12 cm cell:} \quad \frac{150 \text{ wafers}}{\text{tank}} \times \frac{3 \text{ sinks}}{\text{hood}} \times \frac{10 \text{ runs}}{\text{hour}} = \frac{4500 \text{ wafers}}{\text{hour}}$$

The third operation of this process is that of a rinse and dry procedure as is described in Section 4.3.7.6. The shorter time will result in capacities of 1800 wafers/hour and 1200 wafers/hour for 7.6 cm and 12 cm diameter wafers respectively.

Next, photoresist is removed by plasma technology as is described in Section 4 .3.7.18.

Oxide is then removed (operations 5 and 6) utilizing a hood as described in operations 1 and 2 of this process. All physical assumptions and calculations for operations 5 and 6 are the same as those used in operations 1 and 2.

Expense Items

Cost of 5:1:4 HNO_3:Acetic:HF - assume chemicals changed daily

$$= \frac{5\ [\$2.45/\text{gal}\ (HNO_3)] + \$3.95/\text{gal}\ (\text{Acetic}) + 4\ [\$2.90/\text{gal}\ (HF)]}{10} = \frac{\$2.78}{\text{gal}}$$

7.6 cm, 3 tanks: $\frac{6.318\ \text{gal}}{\text{hood}} \times \frac{\$2.78}{\text{gal}} \times \frac{240\ \text{days}}{\text{year}} = \frac{\$4215}{\text{year}} = \frac{\$0.13}{1000\ \text{wafers}}$

12 cm, 3 tanks: $\frac{9.6784\ \text{gal}}{\text{hood}} \times \frac{\$2.78}{\text{gal}} \times \frac{240\ \text{days}}{\text{year}} = \frac{\$6457}{\text{year}} = \frac{\$0.27}{1000\ \text{wafers}}$

Annual cost of 4:1 NH_4F:HF @ \$2.97/gallon using the same calculations as above is:

7.6 cm: \$4503/year = \$0.14/1000 wafers

12 cm: \$6899/year = \$0.28/1000 wafers

Additional expense items include carriers and quartzware which were previously described in Section 4.3.3.7. The costs, assuming 100% equipment utilization, are:

7.6 cm	\$922/year - carriers = \$0.028/1000 wafers
	\$1392/year - quartz = \$0.043/1000 wafers
12 cm	\$1152/year - carriers = \$0.047/1000 wafers
	\$1392/year - quartz = \$0.057/1000 wafers

Facility requirements are:

Electrical	1.1 KW hood (operations 1-2 & 5-6)
	1 KW Rinse-dry
Exhaust	450 CFM Hood (operations 1-2 & 5-6)
DIH_2O	1.6 GPM - Rinse-Dry
	3 GPM - Hood (operations 1-2 & 5-6)

4.3.7.20 STEP 23: DIELECTRIC ETCH (WET)

Capital Equipment Assumptions

Wet chemistry etching of dielectrics utilizes the same hoods described in Section 4.3.7.19. As was stated in that discussion, three tanks will contain etch and three will be used for a short DIH_2O rinse. Cost of this hood is expected to be \$4500; it requires 45 ft^2 and one operator. Assume 10 minutes/batch (load + 1.5 min. etch + unload + 5 min DIH_2O rinse), thus, 6 batches/hour.

7.6 cm cell: $\frac{6 \text{ batches}}{\text{hour}} \times \frac{200 \text{ wafers}}{\text{sink}} \times \frac{3 \text{ tanks}}{\text{batch}} = \frac{3600 \text{ wafers}}{\text{hour}}$

12 cm cell: $\frac{6 \text{ batches}}{\text{hour}} \times \frac{150 \text{ wafers}}{\text{sink}} \times \frac{3 \text{ tanks}}{\text{batch}} = \frac{2700 \text{ wafers}}{\text{hour}}$

Expense Items (assume chemicals changed daily)

7.6 cm cell: $\frac{6.3178 \text{ gal}}{\text{day/hood}} \times \frac{240 \text{ day}}{\text{year}} \times \frac{\$2.97}{\text{gal}} = \frac{\$4503}{\text{year/hood}} = \frac{\$0.23}{1000 \text{ wafers}}$

12 cm cell: $\frac{9.6784 \text{ gal}}{\text{day/hood}} \times \frac{240 \text{ day}}{\text{year}} \times \frac{\$2.97}{\text{gal}} = \frac{\$6899}{\text{year/hood}} = \frac{\$0.47}{1000 \text{ wafers}}$

Other expenses which are explained in Section 4.3.7.7 include:

7.6 cm	\$922/year - carriers	=	\$0.047/1000 wafers
	\$1392/year - quartz	=	\$0.072/1000 wafers
12 cm	\$1152/year - carriers	=	\$0.079/1000 wafers
	\$1392/year - quartz	=	\$0.095/1000 wafers

Facility requirements are:

Electrical	1.1 KW
Exhaust	450 CFM
DIH_2O	3 GPM

4.3.7.21 STEPS 24, 25, 26, 27, 28: ELECTROLESS PLATING

Capital Equipment Assumptions

This process step assumes several independent sequential operations which are outlined below:

1. 10:1 H_2O:HF etch + DIH_2O rinse
2. Sensitize surface
3. Electroless plating (Pd)
4. DIH_2O rinse and dry (centrifuge: Section 4.3.7.6)
5. Sinter
6. 10:1 H_2O:HF etch + DIH_2O rinse
7. Electroless plating (Ni)
8. DIH_2O rinse and dry (centrifuge: Section 4.3.7.6)
9. Sinter

Using this process, the first operation would require a hood as described in Section 4.3.7.7 (excluding the chemical recirculating system) where three of the tanks contain 10:1 H_2O:HF and the remaining three tanks are used for the DIH_2O rinse. (Expense items are the same as discussed in the previous section.) The longest portion of this process is the DIH_2O rinse, which is estimated to be 10 minutes. Since the etch portion of this process is approximately 5 seconds, the total process time will be assumed to be 10 minutes. Five minutes is added for load and unload operations, permitting four cycles/hour.

Thus:

$$\underline{7.6\text{ cm}}: \frac{50\text{ wafers}}{\text{carrier}} \times \frac{4\text{ carriers}}{\text{sink}} \times \frac{3\text{ sinks}}{\text{hood}} \times \frac{4\text{ cycles}}{\text{hour}} = \frac{2400\text{ wafers}}{\text{hood-hour}}$$

$$\underline{12\text{ cm}}: \frac{50\text{ wafers}}{\text{carrier}} \times \frac{3\text{ carriers}}{\text{sink}} \times \frac{3\text{ sinks}}{\text{hood}} \times \frac{4\text{ cycles}}{\text{hour}} = \frac{1800\text{ wafers}}{\text{hood-hour}}$$

The next operation requires sensitize, rinse, and Pd plating steps. Again, using a six sink hood, two sinks can be used for each step. These steps require times of 75 seconds, 10 minutes, and one minute respectively. As above, assuming that four cycles can be performed each hour, a throughput of $\frac{1600\ (7.6\ \text{cm})\ \text{wafers}}{\text{hood-hour}}$ and $\frac{1200\ (12\ \text{cm})\ \text{wafers}}{\text{hood-hour}}$ can be achieved.

Following the first plating operation, a DIH_2O rinse and dry operation is required. For this analysis, the centrifuge step, Section 4.3.7.6, will be utilized.

Once the wafers are rinsed and dried, an anneal must be performed. The most probable cost effective method is to transport the wafers through a furnace on a continuous belt. Assume two carriers, each containing 50 wafers, are placed on a belt. Also, assume the time necessary for these carriers to pass through the furnace is 30 minutes and that two new boats of wafers can be placed on the belt every 30 seconds. After the first 30 minutes, two boats containing a total of 100 wafers will emerge every 30 seconds. This results in a throughput of 200 wafers/minute = 12,000/hour. For this process step, a belt furnace costing $35K and requiring 132 ft^2 is assumed. Each furnace will require an operator.

The next process operations evaluated include an etch, DIH_2O rinse, and electroless Ni plating operation. This is assumed to occur in a hood similar to that described in the sensitize, rinse, and Pd plate operation. The Ni plating operation will take five minutes. This results in only three operations/hour being performed in one hood, resulting in a throughput of 1200 wafers/hour for 7.6 cm diameter wafers and 900 wafers/hour for 12 cm diameter wafers.

Next, a DIH_2O rinse and dry operation, as previously described, is performed.

Finally, a low temperature ($200^{\circ}C$ - $400^{\circ}C$) anneal is accomplished in a belt furnace similar to that already described. For this analysis, a throughput

twice that of the first anneal will be assumed.

Expense and Material Items

The Ni and Pd platings will each cover 100% of the wafer back and 8% of the wafer front from solutions that have a plating efficiency of 35%. The unused Ni solution will not be reclaimed.

The Ni plating solution costs \$0.48/ℓ. Of this, \$0.0157/ℓ is Ni and can be associated with material plated onto the cell. Since 631.5 wafers (7.6 cm diameter) can be plated from a liter of solution, then a material cost of \$0.0249/1000 (7.6 cm diameter) wafers can be identified. The remainder, \$0.4648/ℓ, can be associated with expense items in the Ni plating operation or \$0.74/1000 wafers. Since the plating cost is a direct function of the area being plated and the ratio of plated areas for 7.6 cm diameter cells to 12 cm diameter cells is 2.4931 then the material portion of the nickel operation on a 12 cm diameter cell will be \$0.062/1000 wafers and the expense portion will be \$1.84/1000 wafers.

In the case of the Pd plating operation, the solution cost is \$2.137/ℓ. From this solution, 105 7.6 cm diameter wafers can be plated resulting in a cost of \$20.36/1000 wafers (materials). The unplated Pd remaining in solution is reclaimed at 2/3 original cost resulting in an expense of \$4.13/1000 wafers. Using the area ratio developed above, 12 cm diameter wafers will cost \$50.77/1000 wafers (materials) and \$10.30/1000 wafers (expense).

Additional expense items include those listed in Sections 4.3.7.6 and 4.3.7.7.

Material Items

These costs are shown in the expense calculations above.

4.3.7.22 STEP 29: SOLDER COATING

Capital Equipment Assumptions

This process step assumes an automatic solder system which contains a flux applicator, pre-heater, solderer, and a cleaning and drying section. Including a wafer transport system this apparatus is estimated to cost $50K. Other assumptions include:

- solder fountain width is 15"
- transport speed is 10 ft/min .

Using these assumptions, four 7.6 cm diameter wafers or three 12 cm diameter wafers can be processed simultaneously. If the wafers are transported with one diameter spacing, then $\frac{\text{20 wafers (7.6 cm)}}{\text{min.}} \times 4 \text{ tracks} = \frac{\text{80 wafers}}{\text{min.}} = \frac{\text{4800 wafers}}{\text{hour}}$. Similarly, $\frac{\text{12.7 wafers (12 cm)}}{\text{min.}} \times 3 \text{ tracks} = \frac{\text{38.1 wafers}}{\text{min.}} = \frac{\text{2286 wafers}}{\text{hour}}$.

Expense Items

Facility requirements include:

Electrical	15 KW
Exhaust	4000 CFM
DIH_2O	10 GPM

Flux will coat 200 ft^2/gal = 185,806 cm^2/gal. Since both sides of the wafer must be totally fluxed, areas are 2X single side area. Therefore, 2048 (7.6 cm diameter) wafers and 1643 (12 cm diameter) wafers can be fluxed. At $10/gal:

7.6 cm: $\frac{\$10}{\text{gal}} \times \frac{\text{1 gal}}{\text{2048 wafers}} = \frac{\$4.88}{\text{1000 wafers}}$

12 cm: $\frac{\$10}{\text{gal}} \times \frac{\text{1 gal}}{\text{1643 wafers}} = \frac{\$6.09}{\text{1000 wafers}}$

Material Items

Solder:

$$\frac{\$2.68235/\text{lb}}{180.51\ (7.6\ \text{cm diameter})\ \text{wafers/lb}} = \frac{\$14.86}{1000\ \text{wafers}}$$

Using the ratio of areas, 12 cm diameter wafers will cost $37.04/1000 wafers.

4.3.7.23 STEP 30: ELECTRICAL TEST-CELLS

Capital Equipment Assumptions

This process step requires an automatic wafer transport system, cell alignment stage, data acquisition system, and illumination source. These items are estimated to cost:

.	Wafer transport system	$20K
.	Cell alignment stage	5K
.	Data acquisition	16K
.	Illumination source	1K
.	Temperature controlled stage	4K
	TOTAL	$46K

It is estimated that a cell can be tested in 5 seconds resulting in a throughput of 720 cells per hour. Floor space is 100 ft^2 and one operator is required for each cell test station.

Expense Items

Electrical	2 KW

4.3.7.24 STEPS 31, 32, 33, 34, 35: MODULE FABRICATION

Capital Equipment Assumptions

Equipment assumptions used in this analysis are, in many cases, based on equipment not yet developed. The procedure of panel assembly is listed below:

1. Cell align (aligns and attaches cells by reflow to interconnect substrate)
2. Clean (removes flux)
3. Assembly (places substrate with cells attached into pan, injects silicone, and places glass over cells)
4. Rivet/Weld (attaches bezel)
5. Cure (thermally cures silicone)

Using the process outlined above, the following equipment assumptions are made:

1. Cell Align - For this operation, the interconnect substrate is attached to an indexing X-Y table. Cells are aligned for X, Y and θ and placed on the substrate. Using localized heating, the cell is attached at this time. Following each cell attachment, the X-Y table indexes and another cell is aligned and placed on the substrate. It is anticipated that, by using a hybrid of today's technology equipment, this step can be achieved in this manner. Estimated cost of such a machine is $80K. The area required for such a machine is expected to be 10' X 10'. Including support space, a total area of 200 ft^2 is necessary. Alignment time is assumed to be 5 seconds/cell resulting in a panel alignment time of 20 minutes for 7.6 cm diameter cells (238 cells X 5 sec./cell) and 8.25 minutes for 12 cm diameter cells

(99 cells X 5 sec./cell). Using a cassette fed system, one operator can handle this process step.

2. Clean - After cells are attached by solder reflow to the interconnect substrate, solder flux must be removed. For this process step, assume a belt transport system which will spray a cleaning agent. An aqueous flux is suggested such that the spray can be water. The floor space, throughput, and operator requirements are assumed to be 350 ft^2, 15 panels/hour based on a 5 foot wide belt moving at 1 ft/min., and one operator. Capital cost is estimated to be \$35K.

3. Assembly - Cleaned interconnect substrates containing attached solar cells are placed into a pan assembly, covered with silicone from injector apparatus, and have a glass cover plate placed over the array. It is assumed that an automatic, belt transport system can perform this process at the same rate as described above in a machine requiring 500 ft^2 costing \$55K and requiring one operator.

4. Rivet/Weld - Assembled panels are indexed into an area where a bezel is placed over the panel after a peripheral sealant has been injected. Riveting occurs at a rate of 1 panel/minute = 60 panels per hour. This equipment is estimated to cost \$50K, require 144 ft^2 and one operator.

5. Cure - The final process used in panel assembly is a temperature cure which requires 2 hours. Assume a 6' high oven which is loaded from a belt and will contain 24 panels (2"/panel + 1" space). If a panel can be inserted into the oven in 5 seconds, then 2 minutes are necessary to load the oven (this can be included in the 2 hour cure time). Floor space is estimated to be 25 ft^2 (5' X 5') for the oven plus 400 ft^2 (20' X 20') for staging and loading apparatus plus 175 ft^2 for work area = 600 ft^2 total. It is estimated that the oven will cost \$15K and the load apparatus \$20K, for a total of \$35K. One operator will be required.

Expense Items

Panel Assembly

7.6 cm Item	Cost (K$)	Area (ft^2)	Capacity (PPH)	Power (KW)	Exhaust (CFM)	DIH_2O (GPM)	N_2 (ℓ/m)	Staff (OPI)
Cell Align	80	200	3	1.5	--	--	--	1
Clean	35	350	15	1	400	10	25	1
Assembler	55	500	15	4	400	--	--	1
Riveter	50	144	60	2.5	--	--	--	1
Cure	35	600	12	10	200	--	--	1

The only difference in this equipment and that required for 12 cm diameter cells is in the cell align step where the capacity will be 5.91 PPH (panels per hour).

Material Items

Pan Requirements

- Size: 48" X 48" X .02" = 2304 in^2 X .02" = 46.08 in^3
- Material: Cold rolled steel
- Bezel requirements, four pieces
  - 4 X 2.5" X 48" X .03" = 480 in^2 X .03" = 14.4 in^3

Item	Unit $	7.6 cm $/W	12 cm $/W
Pan	$ 3.2145	.0213	.0205
Bezel	0.8394	.0056	.0054
Coating	2.7937	.0185	.0178
Glass	11.0202	.0729	.0703
Feedthrough	.60	.0040	.0038
Insulator	.092	.0006	.0006
Interconnect	9.6970	.0642	.0619
Silicone	5.4857	.0363	.0350
Gasket	.60	.0040	.0040
TOTAL	$34.3425	.2272	.2191

4.3.7.25 STEP 36: ELECTRICAL TEST - MODULE

Capital Equipment Assumptions

Panel testing is assumed to use a Spectrolab LAPSS pulsed lamp system which costs $80K. Automatic indexing of panels into the test area is expected to add $15K to the equipment cost. A room 8' wide X 22' long is necessary for uniform illumination of a 4' X 4' panel. Additional area for the panel indexing system is expected to require that a total area of 250 ft^2 be provided for this process step. One operator is necessary for this equipment. 15 seconds will be allowed for this operation resulting in a 240 panel/hr rate.

Expense Items

Electrical	2.5 KW

4.3.8 OVERHEAD ASSUMPTIONS

The specific categories which contribute to overhead costs are presented in this section. Each category is itemized; in no case is any category merely taken as a percentage of some quantity, such as labor. Specific categories are presented below:

4.3.8.1 DIRECT FACTORY OVERHEAD

This section includes one foreman per shift and is independent of the range of factory sizes to be evaluated (a conservative assumption). Supervisors are required at one per 15 direct labor personnel in crystal and wafer processing areas and one per 25 direct labor personnel in the panel assembly area. Annual salaries are assumed to be $16K for foreman and $10K for supervisors. Foreman are hired during Phase II and supervisors are added in Phase

III as needed to accommodate the increasing direct labor employment level. Direct factory expense items are listed in a separate expense category.

4.3.8.2 ENGINEERING

The engineering area will maintain process integrity and perform Q.A. functions. The following engineering staff will remain constant over the range of annual production to be evaluated.

(1) Manager @ $23K/year

(3) Engineers @ $20K/year each

(3) Technicians @ $280/week each

Capital equipment is expected to cost $185K and will be depreciated over 8 years on a straight line basis. Associated expenses are assumed to be 25% of the total engineering cost, excluding depreciation. All engineers will be hired in the first phase with technicians being added in Phase II.

4.3.8.3 PRODUCTION CONTROL

Since this factory produces only one product and the number of customers will remain essentially constant, annual production volume will only minimally affect the size of the production control operation. The following personnel will staff this area:

(1) Manager @ $22K/year

(1) Secretary @ $172/week

(1) Scheduler @ $18K/year

(2) Clerks @ $160/week

(1) Customer Service Engineer @ $18K/year

(1) Order Entry Clerk @ $172/week

(4) Inventory Control @ $174/week

This group will remain constant up to 5 MW annual production at which time one inventory control person will be added for each additional 5 MW of annual production. It is assumed that this group will provide warehouse personnel requirements. Capital equipment, depreciated as support equipment, will include fork-lifts, pallet trucks, and the storage racks. Expense items are assumed to be 5% of salaries. Production control will be initiated in Phase III.

4.3.8.4 . BUILDING SERVICES

This cost category includes lighting and HVAC which are estimated to be 48¢/ft^2/month; taxes and insurance which are estimated to be 25.3¢/ft^2/month; and custodial services which are estimated to be 0.118 man/1000 ft^2 @ $180/week. The square footage of the facility is based on the following assumptions. The total area figure (TOTAL.SQ. FT.) presented later in Table 57 represents only that area which is used for direct manufacturing. In order to estimate the cost of the building as well as area related costs, an estimate of the total factory size must be made. These estimates assume:

TOTAL SQ. FT. X 1.3 = DFA (Direct Factory Area)

This additional 30% is included in the overall factory size to account for hallways and storage areas within the manufacturing area.

DFA X 1.2 = FTL (FACTORY TOTAL)

It is assumed that an additional 20% of the manufacturing area is required to warehouse a 30 day product inventory.

FTL X 1.3 = TBA (Total Building Area)

This additional 30% of the total factory area is utilized for all support functions.

The results of this division of area are:

49% = direct manufacturing area

15% = hallway and storage areas within the manufacturing area

13% = warehouse area

23% = support area

Construction costs are assumed to be $\$80/ft^2$ for manufacturing areas and $30/ft for all other areas. The average cost to build a factory is then: $.49 \times (\$80/ft^2) + .51 \times (\$30/ft^2) = \$54.50/ft^2$. Two distinct factory areas are identified in this cost analysis. The first is direct manufacturing area which is determined by adding the areas required for each piece of equipment used in the several production areas. This manufacturing area, listed in Table 57 as TOTAL SQ. FT., represents 49% of the total factory area and, due to the high degree of utility facilitization, construction costs are estimated to be $\$80/ft^2$. The remaining, non-facilitized, support area (i.e., office, warehouse, etc.) represents 51% of the total factory area and can be constructed for an estimated $\$30/ft^2$. Using these ratios of construction costs and factory utilization, an average construction cost of $\$54.50/ft^2$ for the total factory area was determined. In this analysis, the method used to calculate total factory construction costs is to multiply the area required for direct manufacturing by the average construction cost ($54.50) and divide by the percentage of area used for manufacturing (49%). This artificially allocates all of the construction costs to the direct manufacturing area for calculation purposes only, and results in an effective construction cost of $\$111.20/ft^2$ direct manufacturing area. The total construction cost of the factory, thus, is the product of this effective construction cost/ft^2 and the TOTAL SQ. FT. from Table 57.

The cost of industrial property varies significantly throughout the U.S. For example, Phoenix, Arizona has industrial property in the \$12 - 15K/acre range while San Francisco sells similar property for \$95 - 125K/acre. The national average is approximately \$1/ft^2 or \$44K/ acre. In order to achieve an average cost estimate for a solar cell manufacturing plant, \$1/ft^2 will be used in this analysis. Furthermore, it will be assumed that the total area of the building will be 30% of the total property area. Since the manufacturing area (TSQFT) is 49% of the factory and the factory is 30% of the total property, the effective construction costs of \$111.20/ft^2 of direct manufacturing space will be increased to include property by \$6.80 resulting in an effective cost of \$118/manufacturing ft^2. Area calculations are utilized in the building services costs. Factory building costs form the base for the interest and depreciation figures. Building services are initiated in Phase II.

4.3.8.5 MAINTENANCE

Assumptions here are that one administrator at \$30K/year (1st shift only) and one supervisor at \$20K/year per shift for each 10 technicians are employed. Mechanical/electrical technicians at \$15K/year each are determined by the number and type of equipment used. Each type of machine is designated a maintenance coefficient in the data file to determine maintenance technician requirements for a particular process. Expense items are assumed to be 1.5X technician total salary, and material items are assumed to be 1/3 of the total maintenance cost, (payroll + fringes + expense)/3. It is further assumed that the administrator and three supervisors are employed in Phase II with the remaining staff to be added in Phase III.

4.3.8.6 MANAGEMENT

The management section of overhead is assumed to contain a general manager at $50K and four staff members at $30K each. Expenses are 20% of these salaries. The general manager is included in Phase 1, a staff member (finance manager) is added in Phase II, and the remaining staff is added in Phase III.

4.3.8.7 MARKETING/SALES

Due to the small customer base, the staff in this group is assumed to remain constant and to comprise one product marketer and one salesman, each with annual salaries of $20K, and one clerk at $172/week. Expenses are 1/2 of these salaries and commissions are 2.4 X salesman's salary. It is also assumed that there are no applications activities. The product marketer will begin in Phase II with the remaining staff added in Phase III.

4.3.8.8 PURCHASING

The purchasing function is assumed to remain constant with one purchasing agent at $22K/year and expenses of 20% of salary. This category is initiated in Phase I.

4.3.8.9 FINANCE

Finance personnel include one accounts payable clerk, one accounts receivable clerk, and one payroll clerk each at $172/week. Expenses are 20% of salaries. The accounts payable clerk and the payroll clerk are employed in Phase I and the accounts receivable clerk is employed in Phase III. This function is assumed independent of volume.

4.3.8.10 SECRETARY POOL

Two secretaries and two clerks, each with salaries of $172/week, are assumed for this section. Expense items are assumed to exist in the several areas in which these employees work. One secretary begins in Phase I with the remaining three personnel beginning in Phase III.

4.3.8.11 DATA PROCESSING

This operation is constant and utilizes a leased computer and peripheral equipment at $3500/month. The computer will provide inventory tracking, direct labor reporting, reject analysis, and management information services. One programmer/operator at $20K is required. Expenses are assumed to be $10K per year.

4.3.8.12 TRAINING

Training is considered to be one of the most important functions in the overhead section. As a result, one organizer at $22K, nine trainers for crystal growth and wafer processing at $170/week and three trainers for assembly at $170/week will be employed in Phase II to become familiar with equipment and processes. In Phase III, these people perform an extensive training program for direct labor personnel. In Phase IV the training staff is reduced to five trainers in crystal growth and wafer processing and to one in assembly. In both situations, expenses are assumed to be 10% of salaries.

4.3.8.13 PERSONNEL

This section requires one employee in Phase I at $22K with an additional clerk at $170/week to be added in Phase II. Phases III and IV include these

two employees when volume is equal to 10 MW or less plus an additional employee at $22K/year for each additional 10 MW of annual production. Expenses are 10% of salaries. The manager for this section is included in the Management section.

4.3.8.14 CAFETERIA

Equipment for the cafeteria is estimated to cost $60K. Assuming that the cafeteria is self-sustaining and operates at a breakeven point, no labor or expense need be included. Depreciation on the equipment will begin in Phase III.

4.3.8.15 LEGAL

It is assumed that all legal matters will be performed by a contract attorney for $18K/year beginning in Phase I.

4.3.8.16 SECURITY

Security guards will be employed in Phase III on a one employee per shift basis at $170/week.

4.3.8.17 HEALTH

Nurses will begin in Phase III on a one nurse per shift basis at $200/week. Expenses are 10% of salary.

4.3.8.18 FRINGE BENEFITS

For all indirect labor employees, fringe benefits are assumed to be $2.3K/year times the number of employees regardless of salary or grade.

4.3.9 PROCESS YIELD AND MACHINE EFFICIENCY ASSUMPTIONS

The cost of performing any given process step (and the entire process sequence) is, in addition to expenses already defined, heavily dependent upon the yield through each process step. The yield of a given process step is simply defined as the number of acceptable units out of the process step divided by the number of acceptable units started into the process step. If a process step has well defined control ranges and is operated within those ranges, the yield should be 1.00 (or 100%). Since some variations can always be expected outside the control limits (including breakage from handling), the practically observed yields are always less than 1.00. Based upon volume extrapolations from today's known technology, yields have been assumed for each of the individual process steps which could be incorporated into the factory under consideration.

The yield of the overall process sequence is merely the product of the yields of each of the individual process steps in the sequence. A poor yield at any one process step, thus, can dramatically affect the total yield. Further, to obtain 100 units out of the process sequence, the number of units started must be 100 divided by the yield. This, of course, is also true for any individual process step or group of steps. All substrates which are started but which do not finish, thus, are wasted and have a great impact on the cost of a step (and the overall sequence). One of the most cost sensitive sets of assumptions is the set of process yield assumptions. Since these assumptions must be, in fact, estimated, they are more subjective than many of the other assumptions previously discussed. A careful evaluation of the results of this cost analysis must critically evaluate these yield assumptions.

A second set of assumptions which are partially subjective and which also are highly influential on processing costs are related to machine durability. In this analysis, it is assumed that each piece of processing equipment will be broken down and inoperative a certain portion of the time. It is further assumed that the more complex machinery will have more down-time. An ion implanter, therefore, will have significantly more down-time than a chemical exhaust hood.

The process step yield and machine efficiency assumptions are listed in Table 51.

4.3.10 ELECTRICAL AND DI WATER CONSUMPTION ASSUMPTIONS

Electrical consumption in the factory includes the requirements for operation of building services and equipment as well as the specific requirements for heating, ventilating, and air conditioning (HVAC) in each of the processing areas. The total electrical consumption assumes:

(1) Steady-state operation of equipment requires 50% of the name-plate power (a 50% load factor).

(2) Exhaust power is rated at 100% load factor based on 8766 hours per year.

(3) HVAC power is rated at 40% load factor, based on 8766 hours per year.

(4) Lighting requires 4 watts per square foot.

It is further assumed that:

(5) Exhaust power requirement is 0.46 KW/1000 CFM and is assumed to operate continuously.

TABLE 51

PROCESS STEP YIELD AND MACHINE EFFICIENCY ASSUMPTIONS FOR EACH INDIVIDUAL PROCESS STEP.

		PROCESS YIELD%	MACHINE EFFICIENCY
1	CRYSTAL GROWTH	90.00	.90
2	CRYSTAL GRIND	99.90	.90
3	CRYSTAL CROPPING	99.90	.90
4	CRYSTAL SAW	95.00	.90
5	CLEAN-ETCH	99.80	.90
6	CENTRIFUGE	99.80	.96
7	TEXTURE ETCH	99.20	.93
8	COAT-BAKE	99.40	.92
9	ALIGN-EXPOSE	99.80	.94
10	DEVELOP-BAKE	99.40	.92
11	ETCH STOP APPLY	99.40	.92
12	BORON DIFFUSION	99.00	.88
13	PHOSPHORUS DIFF.	99.00	.88
14	DRIVE-IN DIFF.	99.40	.96
15	ION IMPLANT N	99.80	.80
16	ION IMPL-ADV N	99.80	.80
17	SILICON NITRIDE	99.20	.88
18	HI PRESS. SCRUB	99.60	.95
19	PLASMA CLEAN	99.80	.97
20	MESA ETCH 1	99.80	.93
21	MESA ETCH 2	99.80	.93
22	RINSE-DRY	99.80	.96
23	DIELECTRIC ETCH	99.80	.93
24	PLATING ETCH	99.80	.93
25	PD PLATE	99.00	.88
26	NI PLATE	99.00	.88
27	SINTER 1	99.80	.96
28	SINTER 2	99.80	.96
29	SOLDER COAT	99.80	.88
30	CELL TEST	94.80	.95
31	CELL ATTACH	99.70	.88
32	MODULE CLEAN	99.90	.88
33	MODULE ASSEMBLY	99.95	.88
34	RIVET-WELD	99.95	.88
35	CURE	99.95	.97
36	MODULE TEST	99.80	.95
37	ION IMPL-ADV P	99.80	.80
38	ION IMPLANT P	99.80	.80

(6) HVAC requirements must account for:

(a) Equipment heat dissipation equal to 12.5% of name-plate rating and

(b) conditioning of make-up air at 15 KW/1000 CFM.

DI water consumption assumes a 5400 hour work year. Total electrical and DI consumption for each equipment item and for the total factory can now be calculated utilizing these assumptions.

The consumption of electrical and DI water in the factory is dependent upon the particular building service or type of equipment and process step. Consumption can be classed either as continuous or as demand, and costs have been determined for each piece of equipment accordingly.

Many of the building services and pieces of equipment require full time usage of a particular service whether material is being processed or not. For this continuous usage, consumption is equal to the number of pieces of process equipment required, multiplied by both the individual equipment service requirement and the machine efficiency value (presented earlier in the equipment and process step assumptions). Those pieces of equipment that require the usage of a particular service only when material is being processed will use that service at a rate equal to the product of the machine utilization factor and, again, the product of the number of pieces of that equipment, the individual equipment service requirement, and the machine efficiency value. Demand electrical items are then multiplied by 0.616, (5400 work hours/year)/(8766 hours/year), in order that weekends and holidays can be eliminated in determining the total annual electrical consumption. It should be noted that the machine utilization is factored into electrical

and DIH_2O consumption only; exhaust is assumed to operate continuously.

Once totals are established for each facility requirement in each process sequence, annual consumption is determined by multiplying the total by 8766 annual hours for electrical consumption and by 5400 annual work hours for DIH_2O consumption.

4.4 PRELIMINARY RESULTS

During the first month of this cost study, a preliminary analysis was performed utilizing early estimates of cost components. The "first-cut" analysis was intended to identify the basic feasibility of a $2.00/watt solar cell utilizing near term technology while limiting the scope of the study to areas of future interest. These preliminary results of the costing study are shown in Tables 52, 53, and 54. Each table is presented in a matrix form relating the effects of each of three cell sizes analyzed for each of the three specified process sequences. These preliminary results incorporate an assumed annual production volume of 25 megawatts as well as other nominal values for the variable assumptions. It must be realized that the numbers are only relative since assumptions far less sophisticated than described here were utilized for these calculations.

TABLE 52

PRELIMINARY RESULTS FOR PROCESS SEQUENCE TOTAL COST
(Dollars per Watt)

	ION IMPLANT	DIFFUSION	ADVANCED ION IMPLANT
7.6 cm Cells	2.351	1.753	1.410
12 cm Cells	2.012	1.444	1.259
12 cm Half Cells	2.042	1.471	1.286

TABLE 53

PRELIMINARY RESULTS FOR EQUIPMENT CAPITALIZATION
(Millions of Dollars)

	ION IMPLANT	DIFFUSION	ADVANCED ION IMPLANT
7.6 cm Cells	99	30	23
12 cm Cells	79	21	17
12 cm Half Cells	80	22	18

TABLE 54

PRELIMINARY RESULTS FOR FACTORY REQUIREMENTS
(Thousand Square Feet)

	ION IMPLANT	DIFFUSION	ADVANCED ION IMPLANT
7.6 cm Cells	200	74	55
12 cm Cells	156	43	40
12 cm Half Cells	156	48	41

Table 52 shows preliminary results for the costs of the total process sequence. These costs are highest for the smaller, 7.6 cm diameter cells and for today's ion implantation technology, being near \$2.35/watt. For all process sequences, the 12 cm diameter solar cells exhibit the lowest cost. The halved 12 cm diameter cells are more expensive than the whole 12 cm cells due to the operation costs of halving the cells. The fact that half cells can result in a more efficient module packing factor, reducing the effective encapsulation cost/watt, cannot overcome the costs and yield losses associated with the halving operation. Of today's available technologies, the diffusion process sequence is projected to cost less than \$2.00/watt for all cell sizes studied, with the 12 cm cell costs being less than \$1.50/watt. The projected advanced ion implantation process is the most cost favorable, but it is not yet available.

The major reasons for the higher costs associated with the present ion implantation technology are seen from analyzing the information in Tables 53 and 54. Table 54 presents preliminary factory size requirements. The inefficiency of today's ion implanters is reflected in both very heavy capitalization and large floor space projections. Again, the diffusion process sequence compares favorably to present ion implantation technology, while ultimately being

supplanted by an advanced ion implantation technology. Since capital equipment depreciation is a major cost contribution, factory life is extremely important in determining the amount of depreciation per year. This is discussed in detail in a later section of this report.

As a result of this preliminary analysis, further comparison of the 12 cm diameter half-wafer solar cells to the whole 12 cm diameter cells was deemed to be unnecessary. As a result, no further cost analysis was performed on half-wafer cells.

4.5 CALCULATIONS FOR THE COST ANALYSIS

For the calculations in this cost analysis, some of the assumptions common to each evaluation are held constant, while others are treated as variables in order to determine the sensitivity of the results to the assumptions. Parameters which are treated as constants in all calculations include such items as unit chemical costs, labor rates, process step yields, machine capacities, and machine efficiencies. Parameters which are treated as variables are annual production volume, cell efficiency (encapsulated), polycrystalline silicon cost, the length of each of the phases of the factory, interest rate, and electrical power rate. As a result of varying the life of the factory in each phase, the depreciation rate also becomes a variable, assuming complete depreciation by the end of the factory life.

Each of the variable parameters is given a nominal value within its variable range for the calculations. These values have been chosen such that small changes from the nominal value do not result in wide excursions in the final cost. This allows a more valid study of the sensitivity of final costs to variations in cost analysis parameters. The range of each of the variables, and their nominal values, are listed in Table 55. Sample calculations, each based upon a 12 cm diameter solar cell manufactured by a diffusion process at an annual volume of 25 megawatts are presented in the following sections. These calculations are typical of those utilized for all results.

TABLE 55

VARIABLE PARAMETER RANGES AND NOMINAL VALUES

PARAMETER	RANGE	NOMINAL VALUE
Annual Production Volume	0.5 to 100 megawatts	25 megawatts
Cell Efficiency (Encapsulated)	5% to 20%	14%
Polycrystalline Silicon Cost	0 to \$50/Kg	\$25/Kg
Building Phase (Phase I)	6 to 12 months	6 months
Equipment Phase (Phase II)	6 to 12 months	6 months
Labor Phase (Phase III)	6 to 12 months	6 months
Production Phase (Phase IV)	6 to 72 months	60 months
Interest Rate	5% to 15%	7%
Power Rate	2¢ to 25¢/KWH	2.5¢/KWH

4.5.1 CALCULATIONS FOR PROCESS SEQUENCE YIELD

The average hourly solar cell output volume required to meet any given annual production goal can be readily calculated when the solar cell size and efficiency are specified. This hourly number is that which would result from a process with a 100% process yield. Knowing the required output rate and the individual process step yields, the number of solar cells started into any process sequence can be calculated from the cumulative yield of the individual process steps. (The cumulative yield at a given process step is the product of all the individual process step yields including and following that step.) An example of this calculation, for a diffusion process utilizing 12 cm diameter cells at an annual production of 25 megawatts, is shown in the first three columns of Table 56.

4.5.2 YIELDED MACHINE CAPACITY

Having defined both a machine capacity and a machine efficiency in the assumptions, a yielded machine capacity is calculated from the product of the capacity and efficiency. This information is shown in the last three columns of Table 56. The key for the table is:

STEP YLD (%)	=	Step yield (%)
CUM YLD (%)	=	Cumulative Yield (%)
WAFERS PER HR	=	Wafers per hour
MACH EFF	=	Machine Efficiency
MACH CAP	=	Machine Capacity
YIELD CAP	=	Yielded Machine Capacity

TABLE 56

DIFFUSION PROCESS 12.0 CM DIAMETER CELL
25.0 MEGA WATT ANNUAL PRODUCTION 14 % CELL EFFICIENCY

PROCESS STEP	STEP YLD(%)	CUM YLD(%)	WAFERS PER HR	MACH EFF	MACH CAP	YIELD CAP
CRYSTAL GROWTH	90.0	68.8	4250	.90	60	54
CRYSTAL GRIND	99.9	76.4	3825	.90	1612	1451
CRYSTAL CROPPING	99.9	76.5	3821	.90	5796	5216
CRYSTAL SAW	95.0	76.6	3817	.90	34	31
CLEAN-ETCH	99.8	80.6	3627	.90	1368	1231
PLASMA CLEAN	99.8	80.8	3619	.97	600	582
HI PRESS. SCRUB	99.6	80.9	3612	.95	250	237
BORON DIFFUSION	99.0	81.3	3598	.88	125	110
DRIVE-IN DIFF.	99.4	82.1	3562	.96	250	240
ETCH STOP APPLY	99.4	82.6	3540	.92	250	230
DIELECTRIC ETCH	99.8	83.1	3519	.93	2700	2511
CENTRIFUGE	99.8	83.3	3512	.96	400	384
PLASMA CLEAN	99.8	83.4	3505	.97	600	582
TEXTURE ETCH	99.2	83.6	3498	.93	900	837
CENTRIFUGE	99.8	84.3	3470	.96	400	384
PHOSPHORUS DIFF.	99.0	84.4	3463	.88	125	110
ETCH STOP APPLY	99.4	85.3	3428	.92	250	230
COAT-BAKE	99.4	85.8	3408	.92	250	230
ALIGN-EXPOSE	99.8	86.3	3387	.94	200	188
DEVELOP-BAKE	99.4	86.5	3381	.92	250	230
MESA ETCH 1	99.8	87.0	3360	.93	4500	4185
RINSE-DRY	99.8	87.2	3354	.96	1200	1152
PLASMA CLEAN	99.8	87.4	3347	.97	600	582
MESA ETCH 2	99.8	87.5	3340	.93	4500	4185
CENTRIFUGE	99.8	87.7	3333	.96	400	384
PLASMA CLEAN	99.8	87.9	3327	.97	600	582
HI PRESS. SCRUB	99.6	88.1	3320	.95	250	237
SILICON NITRIDE	99.2	88.4	3307	.88	250	220
COAT-BAKE	99.4	89.1	3280	.92	250	230
ALIGN-EXPOSE	99.8	89.7	3261	.94	200	188
DEVELOP-BAKE	99.4	89.8	3254	.92	250	230
DIELECTRIC ETCH	99.8	90.4	3235	.93	2700	2511
PLASMA CLEAN	99.8	90.6	3228	.97	600	582
HI PRESS. SCRUB	99.6	90.8	3222	.95	250	237
PLATING ETCH	99.8	91.1	3209	.93	1800	1674
PD PLATE	99.0	91.3	3202	.88	1200	1056
CENTRIFUGE	99.8	92.2	3170	.96	400	384
SINTER 1	99.8	92.4	3164	.96	12000	11520
NI PLATE	99.0	92.6	3158	.88	900	792
CENTRIFUGE	99.8	93.5	3126	.96	400	384
SINTER 2	99.8	93.7	3120	.96	24000	23040
SOLDER COAT	99.8	93.9	3114	.88	2286	2012
CELL TEST	94.8	94.1	3107	.95	720	684
CELL ATTACH	99.7	99.3	2946	.88	720	634
MODULE CLEAN	99.9	99.6	2937	.88	1485	1307
MODULE ASSEMBLY	99.9	99.7	2934	.88	1485	1307
RIVET-WELD	99.9	99.7	2933	.88	5940	5227
CURE	99.9	99.8	2931	.97	1188	1152
MODULE TEST	99.8	99.8	2930	.95	23760	22572
FINISHED PRODUCT	100.0	100.0	2923			

4.5.3 CALCULATIONS FOR MACHINE COST, LABOR, AND FLOOR SPACE REQUIREMENTS

Results of the previous calculations are used to calculate total equipment requirements from an actual number standpoint as well as capital cost and floor space requirements, Table 57. The equipment (machine) requirements in both decimal and rounded-up (actual) form are shown in this table to illustrate the effect of machine utilization. The actual number of machines required in a particular step is then multiplied by capital cost, labor requirements, and floor space requirements. Similar to the machine data, the labor also represents a rounded-up integer for each step. (Reduction in this one shift labor figure will occur in later calculations utilizing process grouping techniques.) Totals at the bottom of Table 57 show the cost of capital equipment necessary to fabricate product and the necessary floor space to perform this task.

The key for Table 57 is:

# MACH (DEC)	=	Number of machines in decimal form
# MACH (ACT)	=	Number of machines in rounded-up form
K$ MACH	=	Individual machine cost in $1000 units
TOTAL K$	=	Total cost of machines in $1000 units
LABOR MACH	=	Direct labor to operate one machine
TOTAL DL	=	Direct labor, rounded-up, to operate all machines
SQFT MACH	=	Individual machine floor space (ft^2)
TOTAL SQFT	=	Total machine floor space (ft^2)

TABLE 57

DIFFUSION PPOCESS 12.0 CM DIAMETER CELL
25.0 MEGA WATT ANNUAL PPODUCTION 14 % CELL EFFICIENCY

PROCESS STEP	#MACH (DEC)	#MACH (ACT)	K$ MACH	TOTAL K$	LABOP MACH	TOTAL DL	SOFT MACH	TOTAL SOFT
CRYSTAL GPOWTH	78.70	79	125.0	9875	.33	27	49	3871
CRYSTAL GRIND	2.64	3	50.0	150	.25	1	96	288
CRYSTAL CPOPPING	.73	1	8.0	8	1.00	1	40	40
CRYSTAL SAW	123.13	124	35.0	4340	.05	7	40	4960
CLEAN-ETCH	2.95	3	75.0	225	1.00	3	360	1080
PLASMA CLEAN	6.22	7	15.0	105	.50	4	30	210
HI PRESS. SCRUB	15.24	16	56.4	225	.25	4	45	180
BOPON DIFFUSION	32.71	33	65.3	270	.12	5	275	1135
DRIVE-IN DIFF.	14.84	15	65.3	123	.12	2	275	516
ETCH STOP APPLY	15.39	16	59.1	236	.12	2	80	320
DIELECTRIC ETCH	1.40	2	4.5	9	1.00	2	45	90
CENTRIFUGE	9.15	10	2.5	25	.25	3	30	300
PLASMA CLEAN	6.02	7	15.0	105	.50	4	30	210
TEXTURE ETCH	4.18	5	12.0	60	.50	3	45	225
CENTRIFUGE	9.04	10	2.5	25	.25	3	30	300
PHOSPHORUS DIFF.	31.48	32	65.3	262	.12	4	275	1100
ETCH STOP APPLY	14.90	15	59.1	222	.12	2	80	320
COAT-BAKE	14.82	15	59.1	222	.12	2	80	320
ALIGN-EXPOSE	18.02	19	31.3	593	1.00	19	40	760
DEVELOP-BAKE	14.70	15	57.9	218	.12	2	80	320
MESA ETCH 1	.80	1	4.5	4	1.00	1	45	45
RINSE-DRY	2.91	3	2.5	7	.25	1	30	90
PLASMA CLEAN	5.75	6	15.0	90	.50	3	30	180
MESA ETCH 2	.80	1	4.5	4	1.00	1	45	45
CENTRIFUGE	8.68	9	2.5	22	.25	3	30	270
PLASMA CLEAN	5.72	6	15.0	90	.50	3	30	180
HI PRESS. SCRUB	14.01	15	56.4	212	.25	4	45	180
SILICON NITRIDE	15.03	16	65.3	131	.12	2	275	550
COAT-BAKE	14.26	15	59.1	222	.12	2	80	320
ALIGN-EXPOSE	17.35	18	31.3	562	1.00	18	40	720
DEVELOP-BAKE	14.15	15	57.9	218	.12	2	80	320
DIELECTRIC ETCH	1.29	2	4.5	9	1.00	2	45	90
PLASMA CLEAN	5.55	6	15.0	90	.50	3	30	180
HI PRESS. SCRUB	13.59	14	56.4	199	.25	4	45	180
PLATING ETCH	1.92	2	4.5	9	1.00	2	45	90
PD PLATE	3.03	4	4.5	18	1.00	4	45	180
CENTPIFUGE	8.26	9	2.5	22	.25	3	30	270
SINTEP 1	.27	1	35.0	35	1.00	1	132	132
NI PLATE	3.99	4	4.5	18	1.00	4	45	180
CENTRIFUGE	8.14	9	2.5	22	.25	3	30	270
SINTER 2	.14	1	35.0	35	1.00	1	132	132
SOLDEP COAT	1.55	2	50.0	100	1.00	2	100	200
CELL TEST	4.54	5	46.0	230	1.00	5	100	500
CELL ATTACH	4.65	5	80.0	400	1.00	5	200	1000
MODULE CLEAN	2.25	3	35.0	105	1.00	3	350	1050
MODULE ASSEMBLY	2.24	3	55.0	165	1.00	3	500	1500
RIVET-WELD	.56	1	50.0	50	1.00	1	144	144
CURE	2.54	3	35.0	105	1.00	3	600	1800
MODULE TEST	.13	1	95.0	95	1.00	1	250	250
TOTAL				20577		190		27593

4.5.4 GROUPING OF LABOR WITHIN PROCESS CATEGORIES

The direct labor headcount for a single shift, shown in Table 57, is higher than necessary. It can be lowered by grouping processes together to more efficiently utilize available labor. This reduction reflects the fact that while an integral number of machines is necessary, only a fractional number of machines would be necessary to fulfill production requirements. These calculations are shown in Table 58.

The key for Table 58 is:

EQPT UTL (%)	=	Equipment Utilization (%)
LABOR UTL (%)	=	Labor Utilization (%)
LABOR/STEP	=	Labor per step
LABOR (DEC)	=	Direct labor represented in decimal form
LABOR (ACT)	=	Direct labor, next highest integer after factoring for absenteeism and turnover

Equipment utilization is the ratio of the decimal number of machines over the actual number of machines and represents the percentage of time (after factoring of maintenance time) a particular item must operate in order to produce the desired volume. Labor utilization is determined by multiplying the actual number of machines required for a particular step by the labor per machine figure (which was identified in the assumptions) and dividing by the integerized direct labor value from Table 57. Using the assumption that the number of direct labor personnel specified for a particular process step can perform that operation when the equipment is 100% utilized, then the actual labor

TABLE 58

DIFFUSION PROCESS 12.0 CM DIAMETER CELL
25.0 MEGA WATT ANNUAL PRODUCTION 14 % CELL EFFICIENCY

PROCESS GROUPING

PROCESS STEP	EQPT UTL (%)	LABOR UTL (%)	LABOR /STEP	LABOR (DEC)	LABOR (ACT)
CRYSTAL GROWTH					
CRYSTAL GROWTH	99.6	96.2	27	26.0	
CRYSTAL GRIND	87.9	65.9	1	.7	
CRYSTAL CROPPING	73.3	73.3	1	.7	
TOTAL			29	27.4	29
WAFER PREP					
CRYSTAL SAW	99.3	87.9	7	6.2	
CLEAN-ETCH	98.2	98.2	3	2.9	
TOTAL			10	9.1	10
PHOTOLITHOGRAPHY					
ETCH STOP APPLY	96.2	96.2	2	1.9	
DIELECTRIC ETCH	70.1	70.1	2	1.4	
CENTRIFUGE	91.5	76.2	3	2.3	
PLASMA CLEAN	86.0	75.3	4	3.0	
TEXTURE ETCH	83.6	69.7	3	2.1	
ETCH STOP APPLY	99.4	93.2	2	1.9	
COAT-BAKE	98.8	92.6	2	1.9	
ALIGN-EXPOSE	94.8	94.8	19	18.0	
DEVELOP-BAKE	98.0	91.9	2	1.8	
MESA ETCH 1	80.3	80.3	1	.8	
RINSE-DRY	97.0	72.8	1	.7	
PLASMA CLEAN	95.8	95.8	3	2.9	
MESA ETCH 2	79.8	79.8	1	.8	
CENTRIFUGE	96.4	72.3	3	2.2	
COAT-BAKE	95.1	89.1	2	1.8	
ALIGN-EXPOSE	96.4	96.4	18	17.3	
DEVELOP-BAKE	94.3	88.4	2	1.8	
DIELECTRIC ETCH	64.4	64.4	2	1.3	
PLASMA CLEAN	92.4	92.4	3	2.8	
HI PRESS. SCRUB	97.1	85.0	4	3.4	
TOTAL			79	70.0	74
JCT/DIELECT FORM					
PLASMA CLEAN	88.8	77.7	4	3.1	
HI PRESS. SCRUB	95.3	95.3	4	3.8	
BORON DIFFUSION	99.1	81.8	5	4.1	
DRIVE-IN DIFF.	98.9	92.8	2	1.9	
CENTRIFUGE	90.4	75.3	3	2.3	
PHOSPHORUS DIFF.	98.4	98.4	4	3.9	
PLASMA CLEAN	95.3	95.3	3	2.9	
HI PRESS. SCRUB	93.4	87.6	4	3.5	
SILICON NITRIDE	93.9	93.9	2	1.9	
TOTAL			31	27.3	29
METALLIZATION					
PLATING ETCH	95.8	95.8	2	1.9	
PD PLATE	75.8	75.8	4	3.0	
CENTRIFUGE	91.7	68.8	3	2.1	
SINTER 1	27.5	27.5	1	.3	
NI PLATE	99.7	99.7	4	4.0	
CENTRIFUGE	90.5	67.8	3	2.0	
SINTER 2	13.5	13.5	1	.1	
SOLDER COAT	77.4	77.4	2	1.5	
TOTAL			20	15.0	16
ASSEMBLY					
CELL TEST	90.8	90.8	5	4.5	
CELL ATTACH	92.9	92.9	5	4.6	
MODULE CLEAN	74.9	74.9	3	2.2	
MODULE ASSEMBLY	74.8	74.8	3	2.2	
RIVET-WELD	56.1	56.1	1	.6	
CURE	84.8	84.8	3	2.5	
MODULE TEST	13.0	13.0	1	.1	
TOTAL			21	16.9	18
PROCESS TOTAL					176

utilization figure, listed in Table 58, is the product of the figure calculated above and machine utilization. For each process step, the decimal labor requirement is determined by multiplying the labor per step figure from Table 57 by the labor utilization figure in Table 58. To determine the actual direct labor required in a particular process category, the sum of all the individual process steps (decimal labor) within that particular category are multiplied by 1.05 to account for a 5% absentee/turnover rate and rounded up to the next highest integer. The purpose of listing labor requirements in both decimal and rounded-up form is to determine if sufficient personnel exist within a process category to perform the miscellaneous tasks not directly related to the manufacturing of product. Note that equipment utilization should not be confused with the actual percentage of time that a particular piece of equipment is used, but that it represents the percentage of available time that the piece of equipment is used; available time being total time reduced by maintenance, cleaning, and any other time in which equipment cannot be used.

4.5.5 FACILITY REQUIREMENT CALCULATIONS

Facility requirements are calculated for each process step and for the process sequence utilizing the requirements for individual pieces of equipment. The facilities necessary to perform each process step are shown in Table 59.

The key for Table 59 is:

PWR KW (1st)	=	Maximum rated (name-plate) electrical power in kilowatts for one machine.

TABLE 59

DIFFUSION PROCESS 12.0 CM DIAMETER CELL
25.0 MEGA WATT ANNUAL PRODUCTION 14 % CELL EFFICIENCY

PROCESS STEP	IND EQPT FACILITY REQ PWR KW	VENT CFM	WTR GPM	# MACH	PROCESS STEP FACILITY REQ PWR KW	VENT CFM	WTR GPM	MACH EFF	EQPT UTL%
CRYSTAL GROWTH	55	40	.0	79	2399	2843	0	.90	99.6
CRYSTAL GRIND	1	40	.0	3	2	107	0	.90	87.9
CRYSTAL CROPPING	6	100	.0	1	2	89	0	.90	73.3
CRYSTAL SAW	1	0	.0	124	68	0	0	.90	99.3
CLEAN-ETCH	10	600	5.0	3	26	1619	13	.90	98.2
PLASMA CLEAN	1	40	.0	7	5	271	0	.97	88.8
HI PRESS. SCRUB	2	320	3.2	16	8	1215	12	.95	95.3
BORON DIFFUSION	140	125	.0	33	508	453	0	.88	99.1
DRIVE-IN DIFF.	140	125	.0	15	251	224	0	.96	98.9
ETCH STOP APPLY	11	480	.0	16	44	1766	0	.92	96.2
DIELECTRIC ETCH.	1	450	3.0	2	2	837	5	.93	70.1
CENTRIFUGE	1	0	1.6	10	5	0	14	.96	91.5
PLASMA CLEAN	1	40	.0	7	5	271	0	.97	86.0
TEXTURE ETCH	1	500	.0	5	7	2325	0	.93	83.6
CENTRIFUGE	1	0	1.6	10	5	0	13	.96	90.4
PHOSPHORUS DIFF.	140	125	.0	32	492	439	0	.88	98.4
ETCH STOP APPLY	11	480	.0	15	41	1656	0	.92	99.4
COAT-BAKE	11	480	.0	15	41	1656	0	.92	98.8
ALIGN-EXPOSE	1	0	.0	19	15	0	0	.94	94.8
DEVELOP-BAKE	11	480	.0	15	41	1656	0	.92	98.0
MESA ETCH 1	1	450	3.0	1	1	418	2	.93	80.3
RINSE-DRY	1	0	1.6	3	1	0	4	.96	97.0
PLASMA CLEAN	1	40	.0	6	5	232	0	.97	95.8
MESA ETCH 2	1	450	3.0	1	1	418	2	.93	79.8
CENTRIFUGE	1	0	1.6	9	5	0	13	.96	96.4
PLASMA CLEAN	1	40	.0	6	5	232	0	.97	95.3
HI PRESS. SCRUB	2	320	3.2	15	8	1139	12	.95	93.4
SILICON NITRIDE	140	125	.0	16	246	219	0	.88	93.9
COAT-BAKE	11	480	.0	15	41	1656	0	.92	95.1
ALIGN-EXPOSE	1	0	.0	18	15	0	0	.94	96.4
DEVELOP-BAKE	11	480	.0	15	41	1656	0	.92	94.3
DIELECTRIC ETCH	1	450	3.0	2	2	837	5	.93	64.4
PLASMA CLEAN	1	40	.0	6	4	232	0	.97	92.4
HI PRESS. SCRUB	2	320	3.2	14	7	1063	11	.95	97.1
PLATING ETCH	1	450	3.0	2	2	837	5	.93	95.8
PD PLATE	1	450	2.0	4	3	1583	7	.88	75.8
CENTRIFUGE	1	0	1.6	9	4	0	12	.96	91.7
SINTER 1	15	100	.0	1	14	95	0	.96	27.5
NI PLATE	1	450	2.0	4	3	1583	7	.88	99.7
CENTRIFUGE	1	0	1.6	9	4	0	12	.96	90.5
SINTER 2	15	100	.0	1	14	95	0	.96	13.5
SOLDER COAT	15	4000	10.0	2	12	7039	13	.88	77.4
CELL TEST	2	0	.0	5	5	0	0	.95	90.8
CELL ATTACH	11	400	.0	5	28	1759	0	.88	92.9
MODULE CLEAN	1	400	10.0	3	1	1055	19	.88	74.9
MODULE ASSEMBLY	4	400	.0	3	4	1055	0	.88	74.8
RIVET-WELD	2	0	.0	1	0	0	0	.88	56.1
CURE	10	200	.0	3	15	582	0	.97	84.8
MODULE TEST	2	0	.0	1	0	0	0	.95	13.0
TOTAL					4482	41235	190		

VENT CFM	=	Exhaust in cubic feet per minute for one machine
WTR GPM	=	Deionized water in gallons per minute for one machine
# MACH	=	Number of machines required for the process step
PWR KW (2nd)	=	Electrical power in kilowatts for the number of machines in the step (includes machine efficiency, utilization and demand, but not 50% load factor)
VENT CFM	=	Exhaust in cubic feet per minute for the process step
WTR GPM	=	Deionized water in gallons per minute for the process step
MACH EFF	=	Machine efficiency
EQPT UTL %	=	Equipment utilization %

4.5.6 TOTAL EXPENSE AND MATERIAL CALCULATIONS

Utilizing data assumed and calculated previously, expense items for the individual process steps and process sequence can now be calculated.

Table 60 illustrates total incurred expenses, which include process expenses, electrical expenses, and DIH_2O expenses. Also presented in Table 60 are the total material cost items. Process expenses are the sum of all expendable items used in the manufacturing of solar cells. These items include, for example, chemicals, and are calculated by determining the cost

TABLE 60

DIFFUSION PROCESS 12.0 CM DIAMETER CELL
25.0 MEGA WATT ANNUAL PRODUCTION 14 % CELL EFFICIENCY
SILICON = $25.00/KILOGRAM POWER RATE = 2.5 CENTS/KWH

EXPENSE & MATERIAL ITEMS

PROCESS STEP	PROCESS EXP (K$)	ELECT EXP (K$)	WATER EXP (K$)	TOTAL EXP (K$)	MATL (K$)
CRYSTAL GROWTH	2465.0	293.3	.0	2758.3	.0
CRYSTAL GRIND	988.0	.4	.0	988.4	.0
CRYSTAL CROPPING	2201.2	.4	.0	2201.6	.0
CRYSTAL SAW	5791.1	8.2	.0	5799.3	.0
CLEAN-ETCH	342.6	5.5	13.6	361.7	2296.4
PLASMA CLEAN	2.9	1.1	.0	4.0	.0
HI PRESS. SCRUB	.0	2.7	12.9	15.6	.0
BORON DIFFUSION	29.8	61.9	.0	91.7	.0
DRIVE-IN DIFF.	13.2	30.7	.0	43.9	.0
ETCH STOP APPLY	111.4	7.9	.0	119.3	.0
DIELECTRIC ETCH	14.1	1.4	5.6	21.1	.0
CENTRIFUGE	2.6	.7	14.1	17.3	.0
PLASMA CLEAN	2.9	1.0	.0	4.0	.0
TEXTURE ETCH	23.5	4.2	.0	27.6	.0
CENTRIFUGE	2.6	.6	13.9	17.1	.0
PHOSPHOPUS DIFF.	118.1	60.0	.0	178.1	.0
ETCH STOP APPLY	107.9	7.4	.0	115.3	.0
COAT-BAKE	107.3	7.4	.0	114.7	.0
ALIGN-EXPOSE	2.6	1.9	.0	4.4	.0
DEVELOP-BAKE	127.4	7.4	.0	134.8	.0
MESA ETCH 1	7.4	.7	2.8	10.9	.0
RINSE-DRY	.8	.2	4.5	5.5	.0
PLASMA CLEAN	2.5	1.0	.0	3.5	.0
MESA ETCH 2	7.7	.7	2.8	11.2	.0
CENTRIFUGE	2.3	.6	13.4	16.3	.0
PLASMA CLEAN	2.5	.9	.0	3.5	.0
HI PRESS. SCRUB	.0	2.6	12.1	14.6	.0
SILICON NITPIDE	27.8	30.0	.0	57.8	.0
COAT-BAKE	103.3	7.4	.0	110.7	.0
ALIGN-EXPOSE	2.5	1.8	.0	4.3	.0
DEVELOP-BAKE	122.6	7.4	.0	130.0	.0
DIELECTRIC ETCH	13.4	1.4	5.6	20.4	.0
PLASMA CLEAN	2.5	.9	.0	3.4	.0
HI PRESS. SCRUB	.0	2.5	11.2	13.7	.0
PLATING ETCH	6.4	1.4	5.6	13.4	.0
PD PLATE	188.3	2.7	7.1	198.1	877.9
CENTRIFUGE	2.3	.6	12.7	15.6	.0
SINTER 1	1.9	1.9	.0	3.8	.0
NI PLATE	45.2	2.7	7.1	55.0	1.1
CENTRIFUGE	2.3	.6	12.6	15.4	.0
SINTER 2	1.9	1.9	.0	3.8	.0
SOLDER COAT	102.4	11.5	13.7	127.6	622.8
CELL TEST	.0	.6	.0	.6	.0
CELL ATTACH	.0	6.0	.0	6.0	.0
MODULE CLEAN	.0	1.6	19.9	21.5	.0
MODULE ASSEMBLY	.0	2.1	.0	2.1	.0
RIVET-WELD	.0	.1	.0	.1	.0
CURE	.0	2.7	.0	2.7	.0
MODULE TEST	.0	.0	.0	.0	5488.6
TOTAL	13100.0	598.7	191.0	13889.7	9286.7

per 1000 wafers produced multiplied by the number of wafers processed in a particular process step per hour and the number of production hours in a year (5400). Wasted silicon is included in this category. Also included in this category are items which are dependent on the number of machines used as well as items which depend on the number of machines used factored by that machine's efficiency and utility factor. Electrical expense is the product of the total electrical power (as defined in Section 4.3.10), 8766 annual hours, and a variable power rate which is nominally 2½¢/KWH. DIH_2O expense is the product of deionized water consumed per year times $.0031/gallon. Material items are calculated on a per 1000 wafer basis as well as a variable initial silicon cost figure.

The key for Table 60 is:

PROCESS EXP (K$)	=	Process expenses in 1000 dollar units
ELECT EXP (K$)	=	Electrical power expenses in 1000 dollar units
WATER EXP (K$)	=	Deionized water expenses in 1000 dollar units
TOTAL EXP (K$)	=	Total expenses in 1000 dollar units
MATL (K$)	=	Material costs in 1000 dollar units

4.5.7 OVERHEAD CALCULATIONS

Calculations of the overhead associated with each of the four factory phases are presented in Tables 61 through 64. In each phase, the total indirect labor census, payroll, and associated costs are identified. In addition, the indirect expenses, depreciation, interest, materials, and

TABLE 61

DIFFUSION PROCESS 12.0 CM DIAMETER CELL
25.0 MEGA WATT ANNUAL PRODUCTION 14 % CELL EFFICIENCY
DIRECT LABOR CENSUS = 528 POWER RATE = 2.5 CENTS/KWH

OVERHEAD (K$) PHASE 1 = 6 MONTHS

	CENSUS	PAYROLL	FRINGE	EXP	DEP	MAT	COM	TOTAL
DIRECT FACTORY	0	.0	.0	.0	.0	.0	.0	.0
ENGINEERING	4	46.0	4.6	16.8	.0	.0	.0	67.4
PRODUCTION CONT	0	.0	.0	.0	.0	.0	.0	.0
BLDG SERVICES	0	.0	.0	.0	.0	.0	.0	.0
MAINTENANCE	0	.0	.0	.0	.0	.0	.0	.0
MANAGEMENT	1	25.0	1.1	5.0	.0	.0	.0	31.1
MARKETING/SALES	0	.0	.0	.0	.0	.0	.0	.0
PURCHASING	1	11.0	1.1	2.2	.0	.0	.0	14.3
FINANCE	2	19.4	2.3	3.9	.0	.0	.0	25.6
SECRETARY POOL	1	4.4	1.1	.0	.0	.0	.0	5.6
DATA PROCESSING	0	.0	.0	.0	.0	.0	.0	.0
TRAINING	0	.0	.0	.0	.0	.0	.0	.0
PERSONNEL	1	11.0	1.1	1.1	.0	.0	.0	13.2
CAFETERIA	0	.0	.0	.0	.0	.0	.0	.0
LEGAL	0	.0	.0	9.0	.0	.0	.0	9.0
SECURITY	0	.0	.0	.0	.0	.0	.0	.0
HEALTH	0	.0	.0	.0	.0	.0	.0	.0
TOTAL	10	116.9	11.5	38.0	.0	.0	.0	166.4

TABLE 62

DIFFUSION PROCESS 12.0 CM DIAMETER CELL
25.0 MEGA WATT ANNUAL PRODUCTION 14 % CELL EFFICIENCY
DIRECT LABOR CENSUS = 528 POWER RATE = 2.5 CENTS/KWH

OVERHEAD (K$) PHASE 2 = 6 MONTHS

	CENSUS	PAYROLL	FRINGE	EXP	DEP	MAT	COM	TOTAL
DIRECT FACTORY	3	24.0	3.4	.0	.0	.0	.0	27.4
ENGINEERING	7	67.8	8.1	25.3	.0	.0	.0	101.2
PRODUCTION CONT	0	.0	.0	.0	.0	.0	.0	.0
BLDG SERVICES	1	4.7	1.1	247.7	.0	.0	.0	253.5
MAINTENANCE	4	45.0	4.6	5.0	.0	.0	.0	54.6
MANAGEMENT	2	40.0	2.3	8.0	.0	.0	.0	50.3
MARKETING/SALES	1	10.0	1.1	5.0	.0	.0	.0	16.1
PURCHASING	1	11.0	1.1	2.2	.0	.0	.0	14.3
FINANCE	2	19.4	2.3	3.9	.0	.0	.0	25.6
SECRETARY POOL	1	4.4	1.1	.0	.0	.0	.0	5.6
DATA PROCESSING	0	.0	.0	.0	.0	.0	.0	.0
TRAINING	13	64.0	14.9	6.4	.0	.0	.0	85.4
PERSONNEL	2	22.0	2.3	2.2	.0	.0	.0	26.5
CAFETERIA	0	.0	.0	.0	.0	.0	.0	.0
LEGAL	0	.0	.0	9.0	.0	.0	.0	9.0
SECURITY	0	.0	.0	.0	.0	.0	.0	.0
HEALTH	0	.0	.0	.0	.0	.0	.0	.0
TOTAL	37	312.5	42.5	314.7	.0	.0	.0	669.7

TABLE 63

DIFFUSION PPOCESS 12.0 CM DIAMETER CELL
25.0 MEGA WATT ANNUAL PPODUCTION 14 % CELL EFFICIENCY
DIPECT LABOP CENSUS = 528 POWER RATE = 2.5 CENTS/KWH

OVERHEAD (K$) PHASE 3 = 6 MONTHS

	CENSUS	PAYPOLL	FRINGE	EXP	DEP	MAT	COM	TOTAL
DIPECT FACTOPY	30	159.0	34.5	.0	.0	.0	.0	193.5
ENGINEERING	7	67.8	8.1	25.3	11.6	..0	.0	112.7
PPODUCTION CONT	15	82.3	17.2	3.3	6.2	.0	.0	109.1
BLDG SERVICES	7	32.9	8.0	247.7	.0	.0	.0	288.6
MAINTENANCE	106	832.5	121.9	1046.2	.0	666.9	.0	2667.5
MANAGEMENT	5	85.0	6.0	17.0	.0	.0	.0	108.0
MARKETING/SALES	3	24.4	3.4	12.2	.0	.0	14.0	54.1
PUPCHASING	1	11.0	1.1	2.2	.0	.0	.0	14.3
FINANCE	3	13.3	3.4	2.7	.0	.0	.0	19.5
SECPETAPY POOL	4	17.9	4.6	.0	.0	.0	.0	22.5
DATA PPOCESSING	1	10.0	1.1	26.0	.0	.0	.0	37.1
TRAINING	13	64.0	14.9	6.4	.0	.0	.0	85.4
PERSONNEL	4	37.4	4.6	3.7	.0	.0	.0	45.7
CAFETEPIA	0	.0	.0	3.7	.0	.0	.0	3.7
LEGAL	0	.0	.0	9.0	.0	.0	.0	9.0
SECURITY	3	13.2	3.4	.0	.0	.0	.0	16.7
HEALTH	3	15.6	3.4	1.5	.0	.0	.0	20.6
TOTAL	205	1466.6	236.0	1407.1	17.8	666.9	14.0	3808.4

TABLE 64

DIFFUSION PPOCESS 12.0 CM DIAMETER CELL
25.0 MEGA WATT ANNUAL PPODUCTION 14 % CELL EFFICIENCY
DIPECT LABOR CENSUS = 528 POWEP PATE = 2.5 CENTS/KWH

OVERHEAD (K$) PHASE 4 = 60 MONTHS

	CENSUS	PAYROLL	FRINGE	EXP	DEP	MAT	COM	TOTAL
DIPECT FACTOPY	42	2190.0	483.0	.0	.0	.0	.0	2673.0
ENGINEEPING	7	678.5	80.5	253.0	115.5	.0	.0	1127.5
PRODUCTION CONT	15	823.5	172.5	32.9	62.5	.0	.0	1091.4
BLDG SERVICES	7	329.0	80.5	2476.6	.0	.0	.0	2886.1
MAINTENANCE	106	8325.0	1219.0	10462.5	.0	6668.8	.0	26675.3
MANAGEMENT	5	850.0	60.0	170.0	.0	.0	.0	1080.0
MAPKETING/SALES	3	244.5	34.5	122.5	.0	.0	140.0	541.5
PUPCHASING	1	110.0	11.5	22.0	.0	.0	.0	143.5
FINANCE	3	133.5	34.5	27.0	.0	.0	.0	195.0
SECRETARY POOL	4	179.0	46.0	.0	.0	.0	.0	225.0
DATA PPOCESSING	1	100.0	11.5	260.0	.0	.0	.0	371.5
TPAINING	7	375.0	80.5	37.5	.0	.0	.0	493.0
PEPSONNEL	4	374.0	46.0	37.4	.0	.0	.0	457.4
CAFETEPIA	0	.0	.0	37.5	.0	.0	.0	37.5
LEGAL	0	.0	.0	90.0	.0	.0	.0	90.0
SECUPITY	3	132.5	34.5	.0	.0	.0	.0	167.0
HEALTH	3	156.0	34.5	15.5	.0	.0	.0	206.0
TOTAL	211	15000.5	2429.0	14044.4	178.0	6668.8	140.0	38460.7

sales costs are identified for each phase and for each overhead category.

4.5.8 CALCULATION SUMMARY

For each phase, the computer program allows a variable time input.

A summary of costs for each of the four phases is shown in Table 65. Included in this table are material, expense, labor, overhead, interest, and depreciation for each phase. Totals of costs within each phase, totals of costs within a category for all four phases, and a total cost for the life of the factory are included in this table. This information is listed in actual K$, $/W, and percent of total cost for each category. Additionally, the selling price* is determined by:

$$\text{Selling price (\$/Watt)} = \frac{\text{Total Cost}}{\text{Total Watts Produced} \times .85}$$

$$\text{Where Total Watts Produced} = \left(\frac{\text{Phase IV Months}}{\text{12 months}} \times \frac{\text{.25 Phase III Months}}{\text{12 months}}\right)$$
$$\times \text{ Annual Watts Produced.}$$

Three further assumptions are that the manufacturer is in a 50% tax bracket, after tax profit is 7.5%, and 25% of the annual production rate is realized in Phase III.

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*It is recognized that different methods of determining profit can be utilized in these calculations. Accordingly, it has been left as the last calculation. The reader can, if he chooses, utilize the manufacturing cost value presented in Table 65 to calculate a selling price based upon his own method of profit determination.

TABLE 65*

DIFFUSION PROCESS 12.0 CM DIAMETER CELL
25.0 MEGA WATT ANNUAL PRODUCTION 14 % CELL EFFICIENCY
SILICON = $25.00/KILOGRAM POWER RATE = 2.5 CENTS/KWH
DIRECT LABOR CENSUS = 528 INTEREST RATE = 7.0 %

SUMMARY (K$)

FACTORY LIFE		MAT	EXP	LAB	OVR	INT	DEP	TOTAL
PHASE 1	6 MO	0	0	0	166	64	0	231
PHASE 2	6 MO	0	30	0	670	532	38	1270
PHASE 3	6 MO	2322	3472	1956	3808	1169	1998	14726
PHASE 4	60 MO	46434	69449	29172	38461	6654	19981	210150
TOTAL COST		48755	72951	31127	43105	8420	22018	226376
TOTAL	$/WATT	.3805	.5694	.2429	.3364	.0657	.1718	1.7668
		21.5	32.2	13.8	19.0	3.7	9.7	100.0

SELLING PRICE = 2.08 $/WATT

*In the previously distributed Quarterly Report No. 6, an error had been made in the interest calculation. The error made the interest too high by nearly a factor of 3, resulting in the total cost being approximately 5.6% too high. This error has been corrected in the present calculations.

4.6 RESULTS AND DISCUSSION

Results of the cost analysis are presented in this section. The results are shown in graphical form, and illustrate a sensitivity analysis of major cost parameters.

Due to the breadth of assumptions and variables incorporated into this analysis, erroneous conclusions could be drawn if a single value of cost for a manufacturing process were given. Accordingly, the results presented here examine the sensitivity to a group of important variable parameters. These parameters, presented earlier in Table 55, are the cell size, the manufacturing process, the cost of polycrystalline silicon, the encapsulated solar cell efficiency, the interest rate on borrowed money, the electrical power rate, the annual production volume, and the effect of production phase duration. Each of these parameters was assigned a nominal value, chosen such that the overall cost was relatively insensitive to small changes in this (nominal) value. Each of these parameters was individually varied over a broad range of values while all other parameters were held constant at their nominal values, allowing examination of cost sensitivity to the individual parameters.

Specific results for a given set of assumptions may, of course, still be obtained from the data. Such specific results must be viewed with the caveat that the result is only as accurate as the input assumptions. The absolute value of the cost data will change as a function of the assumptions. The trend of the costs, as a function of the key parameters varied here, is the most important information in the presented data, with the absolute value of the data being considered as being within an error band dependent upon the assumptions.

Each of the cost sensitivity graphs has costs plotted as a function of two solar cell diameters, 7.6 cm and 12 cm, for the chosen diffusion process sequence. It is reasonable to assume that the true costs will fall within the range of these two cost curves. In addition to the diffusion process sequence curves, a curve is also shown for the advanced ion implantation process sequence, incorporating an ion implanter yet to be developed. This curve is probably the lower bound for manufacturing costs for the 1982 time-frame. On each graph, the nominal value of the varied parameter is indicated by a dashed line.

A reminder is necessary at this time. A major cost assumption dealt with technology readiness for this study for the 1982 time-frame. This assumption limits the technology and automation of the process to essentially the present status. This cost analysis, thus, should not be utilized to make projections for 1985 and beyond! There should be no concern, thus, that $0.50/watt is not shown on the curves presented here.

4.6.1 INFLATION FACTORS AND COST/PRICE CONSIDERATION

The present cost analysis is being performed with the most current technology and equipment information. Accordingly, all prices and costs used here reflect dollars with mid-1977 values. These, of course, can be directly compared only to other mid-1977 cost analyses unless a scaling factor to adjust for inflation is utilized. The dollar value basis for the LSSA Project is in 1975 dollars, and is defined as the value of dollars on January 1, 1975. A generalized inflation factor, which lumps all cost categories together, has been defined and is listed in Table 66. Accordingly, to arrive at approximate 1975 dollars, the costs identified in this study may be divided by a factor between 1.156 and 1.17. Different cost factors have inflated at different rates,

TABLE 66

LSSA PRICE DEFLATOR TABLE
DATED FOR 1978

QUARTER	1975	1976	1977	1978
1	1.024	1,081	1,136	1.198 (C)
2	1.036	1.094	1.156	1.211 (C)
3	1,053	1.107	1.170	1,230 (C)
4	1,071	1.121	1,183 (C)	---

For a given year and quarter divide price by that number in table. Result = that price in January 1, 1975 dollars.

C = extrapolations

however, giving only an approximate value for the 1975 reference if such a factor is utilized. A precise adjustment would require different inflation adjustments for each individual cost item in labor, materials, overhead, etc. Since this cost analysis has many assumptions and, as specified earlier, is intended primarily to show sensitivity to certain important cost parameters, it has not been deemed fruitful to try to incorporate the additional complexity associated with utilizing such precise inflation adjustments. Further, due to its imprecise nature, the general inflation factor from Table 66 has not been utilized in this study. Accordingly, the cost data reported here are in mid-1977 dollars. Inflation adjustments are left to the reader.

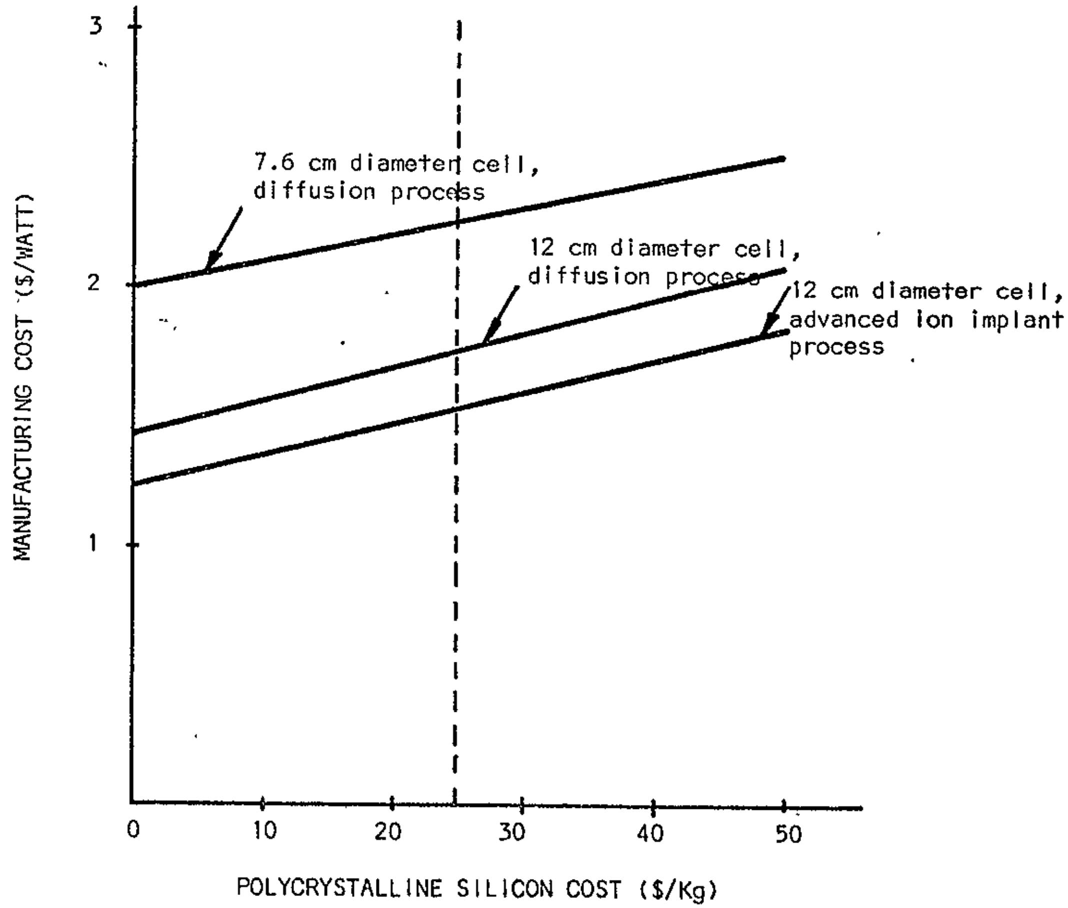
The reader is reminded that data presented here are manufacturing cost data, while goals are selling price figures. The cost will be less than the price by an amount equal to the pretax profit. Since, in addition, the costs reported here are in mid-1977 dollars and price goals are quoted in 1975 dollars, confusion may arise in later discussions. It is suggested that, within the accuracy of the other assumptions, the pretax profit may be considered to be approximately equal to the deflator factor between 1975 and mid-1977 dollars. In this case, the data presented here as costs can be considered as comparable to 1975-based prices.

4.6.2 EFFECT OF POLYCRYSTALLINE SILICON COST ON MANUFACTURING COST

The effect of varying the cost of polycrystalline silicon over the range of zero to $50/Kg is shown in Figure 9. The relation is linear against the manufacturing cost. For the smaller, 7.6 cm diameter solar cell and the nominal fixed values of the other parameters, the manufacturing cost is greater than $2.00/watt at all prices of polycrystalline silicon. For these same nominal values a polycrystalline silicon cost of near $40/Kg can result in a manu-

FIGURE 9. EFFECT OF POLYCRYSTALLINE SILICON COST ON MANUFACTURING COST

Annual Production Volume = 25 Megawatts
Encapsulated Cell Efficiency = 14%
Building Phase = 6 Months
Equipment Phase = 6 Months
Labor Phase = 6 Months
Production Phase = 5 Years
Interest Rate = 7%
Power Rate = 2.5¢/KWH
Cost Reference = Mid-1977 Dollars



facturing cost of less than $2.00/watt for 12 cm diameter solar cells produced by a diffusion process.

4.6.3 EFFECT OF ENCAPSULATED CELL EFFICIENCY ON MANUFACTURING COST

The manufacturing cost is heavily dependent upon encapsulated solar cell efficiency, as shown in Figure 10. As the efficiency increases, such categories as labor, encapsulation materials, and capital investment (especially in the crystal growth area) decrease rapidly. At the nominal values cited, the diffusion process sequence requires greater than a 13% encapsulated cell efficiency for the larger diameter cell to achieve $2.00/watt manufacturing cost.

4.6.4 EFFECT OF INTEREST RATE ON MANUFACTURING COST

Over the broad range of interest rates from 5% to 15%, the manufacturing cost for solar cells changes by less than 15%, Figure 11. The manufacturing cost, thus, is relatively insensitive to this parameter when compared with sensitivities to other parameters.

4.6.5 EFFECT OF ELECTRICAL POWER RATE ON MANUFACTURING COST

The manufacturing cost of solar cell modules is, over a wide range of power rates, quite insensitive to the electrical power rate. Analysis ranging from 2 cents per kilowatt hour to 25 cents per kilowatt hour, shown in Figure 12, indicates only an approximate 10% change in manufacturing cost between extremes of the range. The manufacturing cost is least sensitive to this important parameter (of all the parameters studied for sensitivity).

4.6.6 EFFECT OF ANNUAL PRODUCTION VOLUME ON MANUFACTURING COST

Manufacturing costs are extremely sensitive to annual production volume as seen in Figure 13. Manufacturing costs cannot approach $2.00/watt until

FIGURE 10. EFFECT OF ENCAPSULATED CELL EFFICIENCY ON MANUFACTURING COST

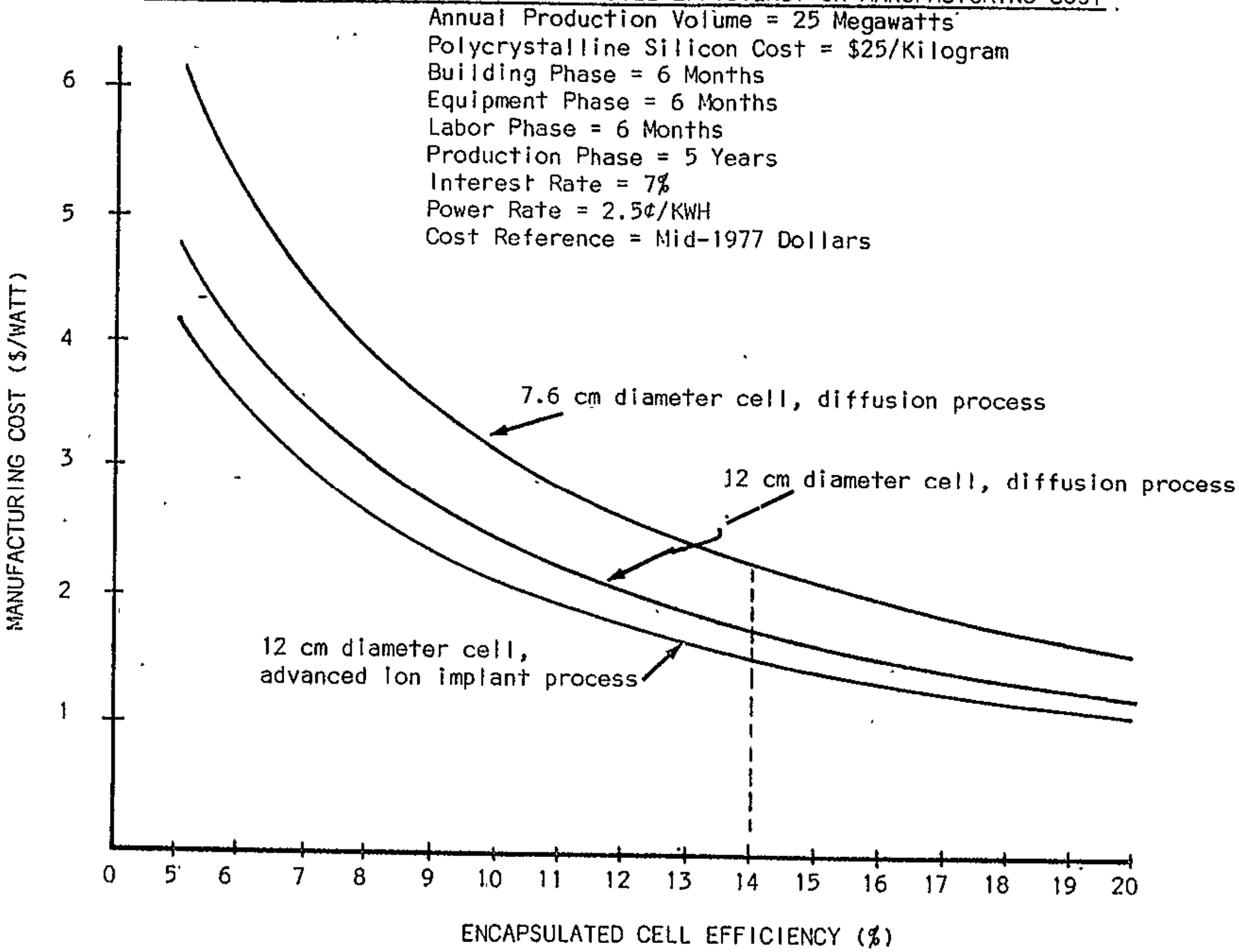


FIGURE 11. EFFECT OF INTEREST RATE ON MANUFACTURING COST

Annual Production Volume = 25 Megawatts
Encapsulated Cell Efficiency = 14%
Building Phase = 6 Months
Equipment Phase = 6 Months
Labor Phase = 6 Months
Production Phase = 5 Years
Interest Rate = 7%
Power Rate = 2.5¢/KWH
Cost Reference = Mid-1977 Dollars

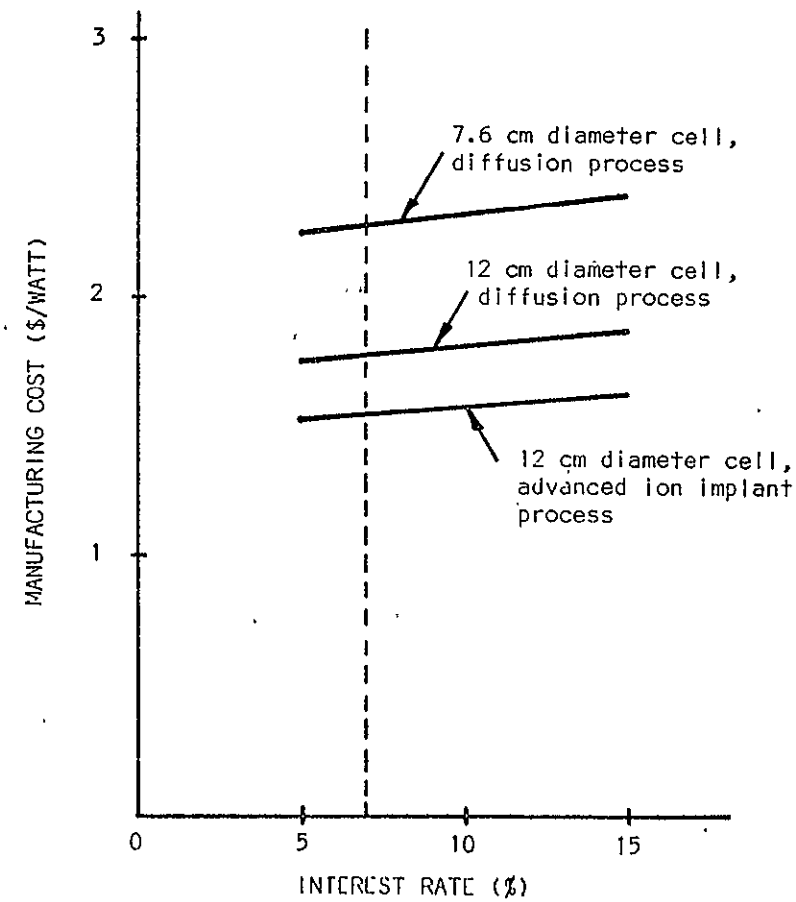
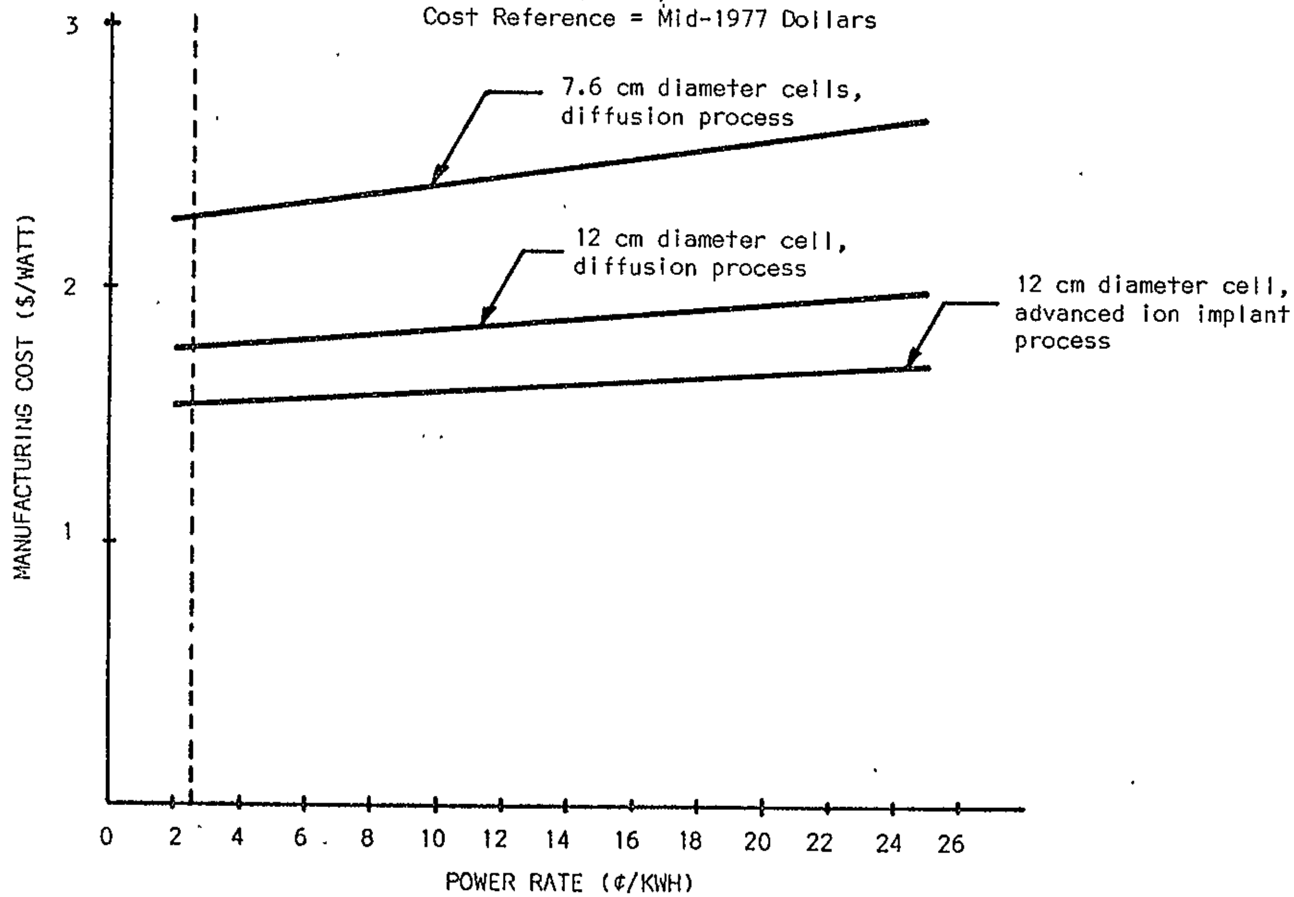


FIGURE 12. EFFECT OF ELECTRICAL POWER RATE ON MANUFACTURING COST

Annual Production Volume = 25 Megawatts
Encapsulated Cell Efficiency = 14%
Polycrystalline Silicon Cost = $25/Kilogram
Building Phase = 6 Months
Equipment Phase = 6 Months
Labor Phase = 6 Months
Production Phase = 5 Years
Interest Rate = 7%
Cost Reference = Mid-1977 Dollars



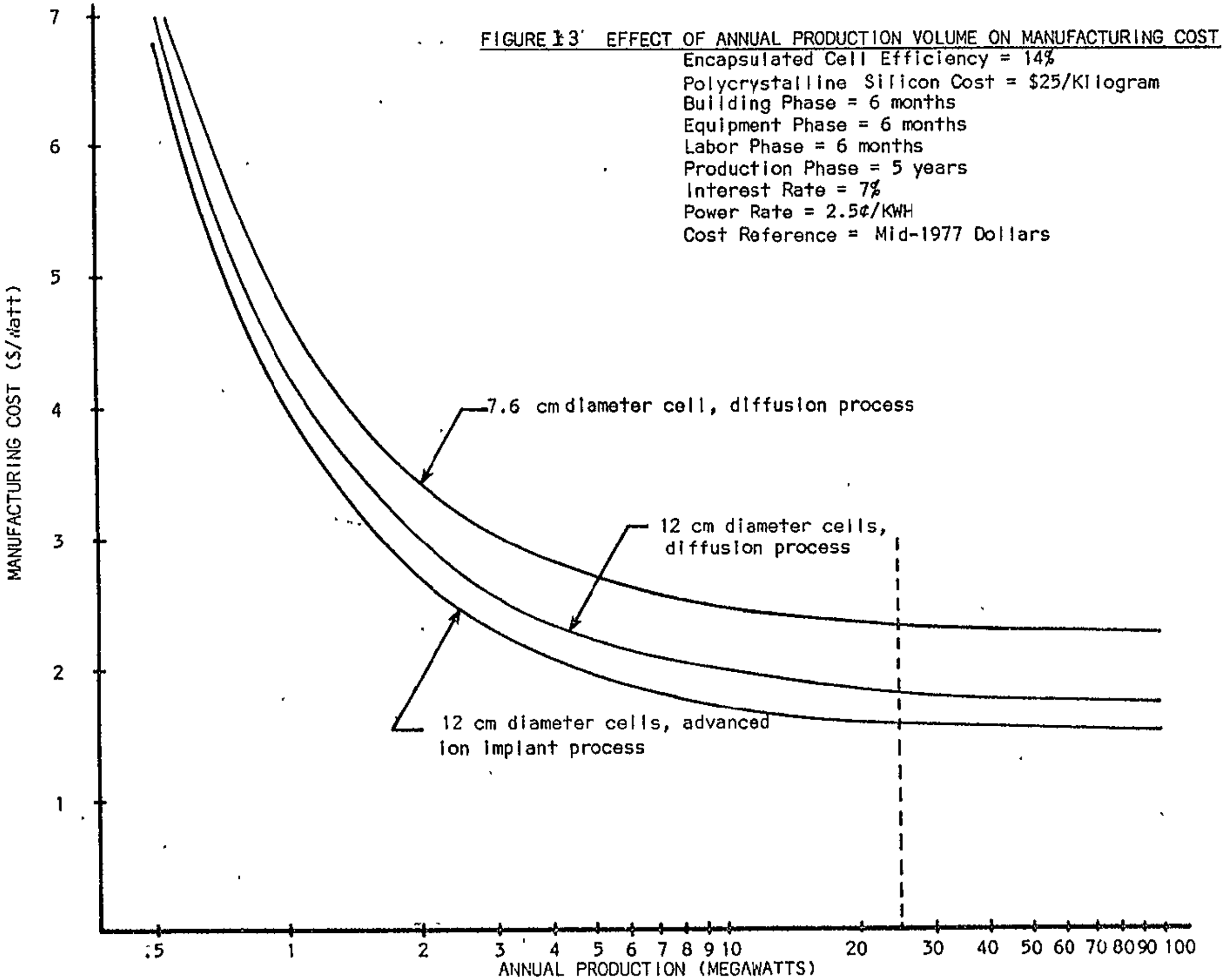


FIGURE 13 EFFECT OF ANNUAL PRODUCTION VOLUME ON MANUFACTURING COST

annual volumes above 5 megawatts are achieved. The cost category contributors to this large production volume sensitivity are illustrated in Figures 14 and 15 for the 12 cm diameter cell manufactured by the diffusion sequence. Figure 14 plots each cost category as a function of the dollar contribution, while Figure 15 replots the same data for each cost category as a percent of the total cost. The manufacturing cost sensitivity is overwhelmingly predominated by one cost category: overhead. The overhead assumptions, Section 4.3.8 indicate that there are certain fixed costs which must be diluted with volume to reduce costs.

Beyond the overhead contribution, the interest, depreciation, and labor cost categories indicate more efficient labor, factory, and equipment utilization with increased volume (an expected result). Expense and material items predominate at increased volumes, requiring reductions in consumed materials to reduce long range costs.

4.6.7 EFFECT OF FACTORY LIFE ON MANUFACTURING COSTS

The duration of the production phase of factory life is very influential on manufacturing costs, while the duration of the building, equipment, and labor phases is much less significant. These factors are plotted in Figure 16 for each of the three size-process sequence combinations shown in previous figures. The production phase must be at least of 3 years duration to approach \$2.00/watt manufacturing costs.

Contribution of individual cost categories to the total cost are shown for the 12 cm cell manufactured by the diffusion process in Figure 17 as actual cost contributors, and in Figure 18 as a percentage of the total cost. For short factory production times, depreciation is the dominant cost factor. This reflects the fact that equipment must be fully depreciated by the end of

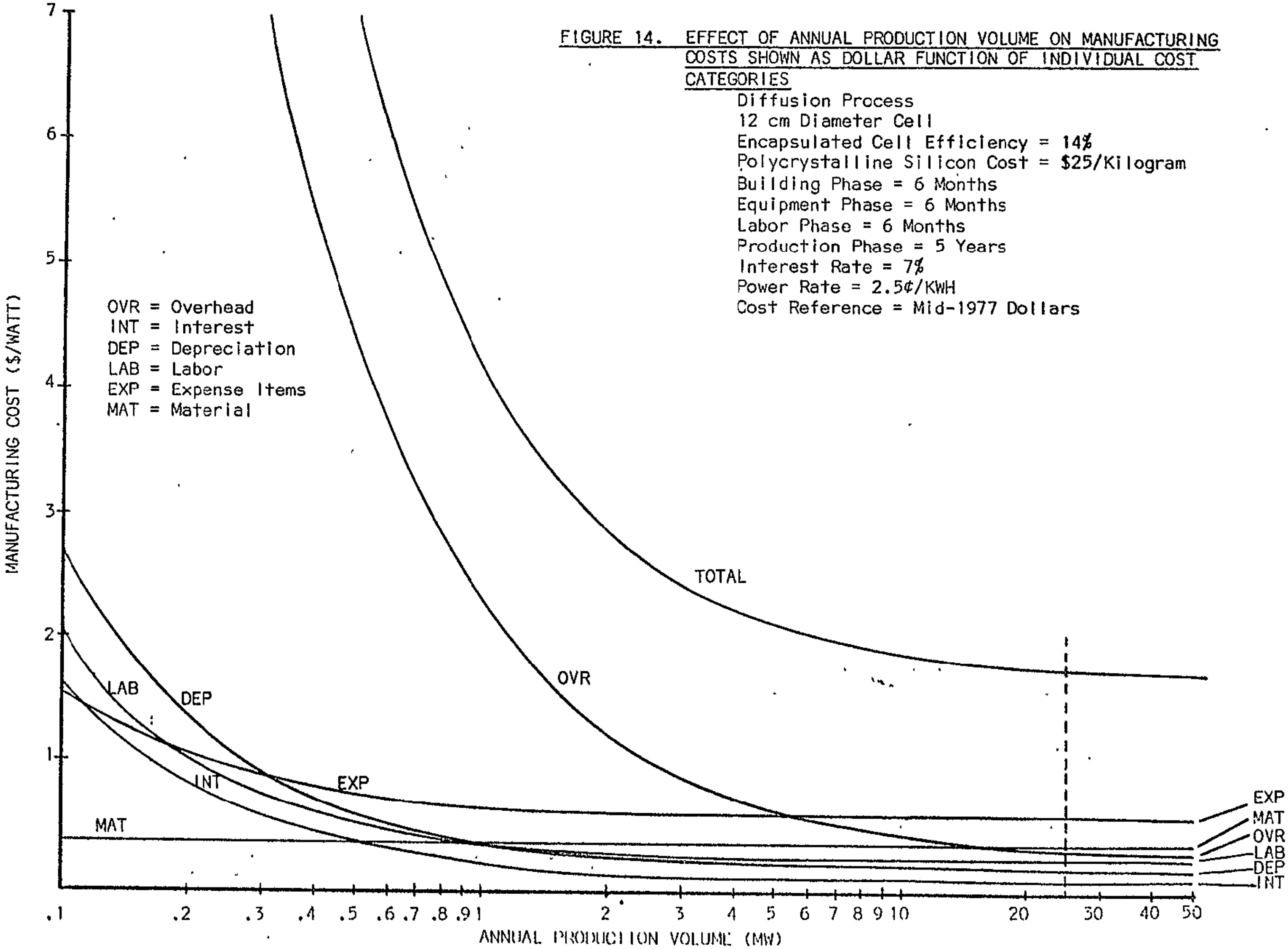


FIGURE 14. EFFECT OF ANNUAL PRODUCTION VOLUME ON MANUFACTURING COSTS SHOWN AS DOLLAR FUNCTION OF INDIVIDUAL COST CATEGORIES

Diffusion Process
12 cm Diameter Cell
Encapsulated Cell Efficiency = 14%
Polycrystalline Silicon Cost = $25/Kilogram
Building Phase = 6 Months
Equipment Phase = 6 Months
Labor Phase = 6 Months
Production Phase = 5 Years
Interest Rate = 7%
Power Rate = 2.5¢/KWH
Cost Reference = Mid-1977 Dollars

FIGURE 15 EFFECT OF ANNUAL PRODUCTION ON MANUFACTURING COSTS SHOWN AS PERCENT CONTRIBUTION OF INDIVIDUAL COST CATEGORIES

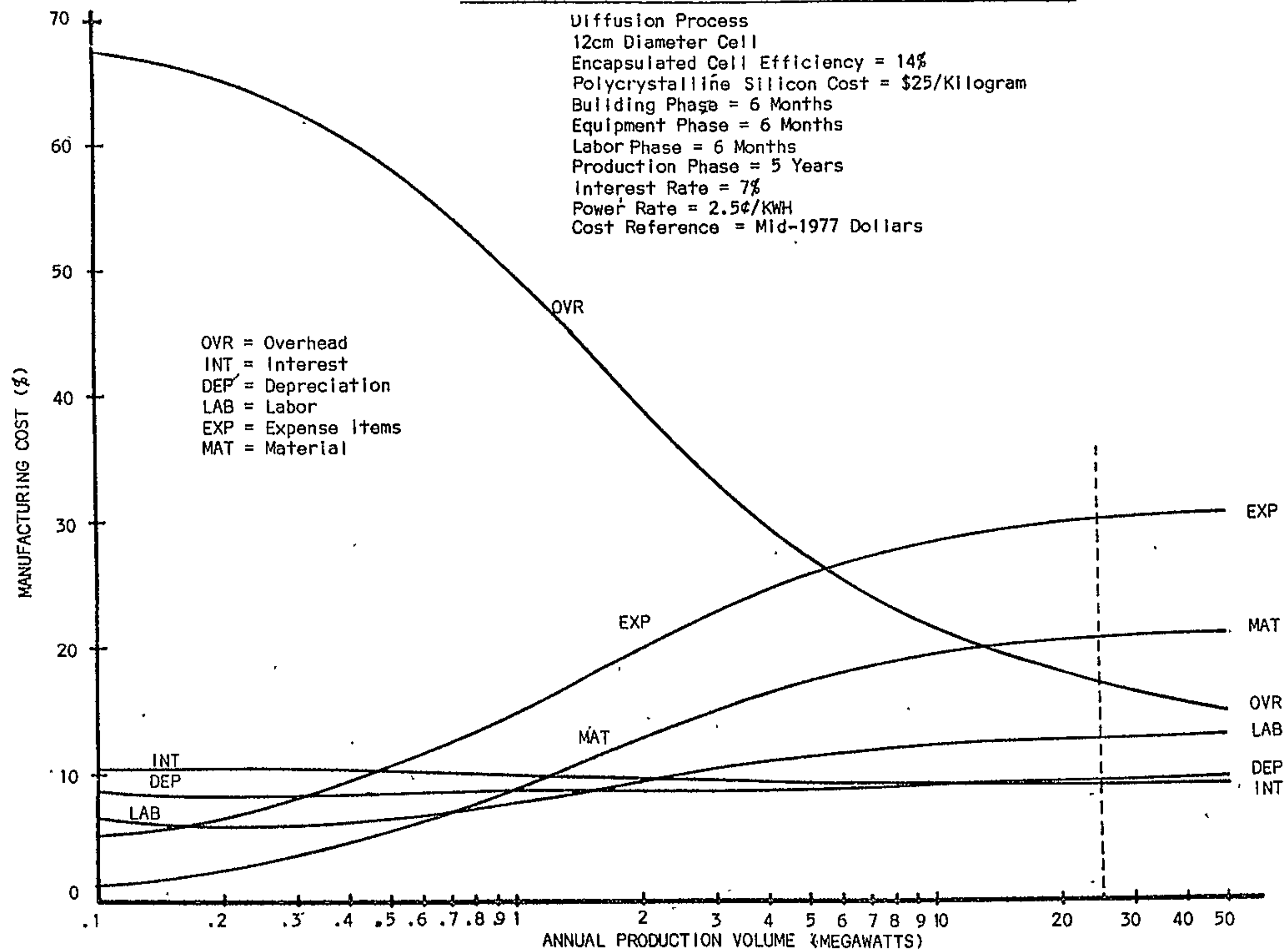
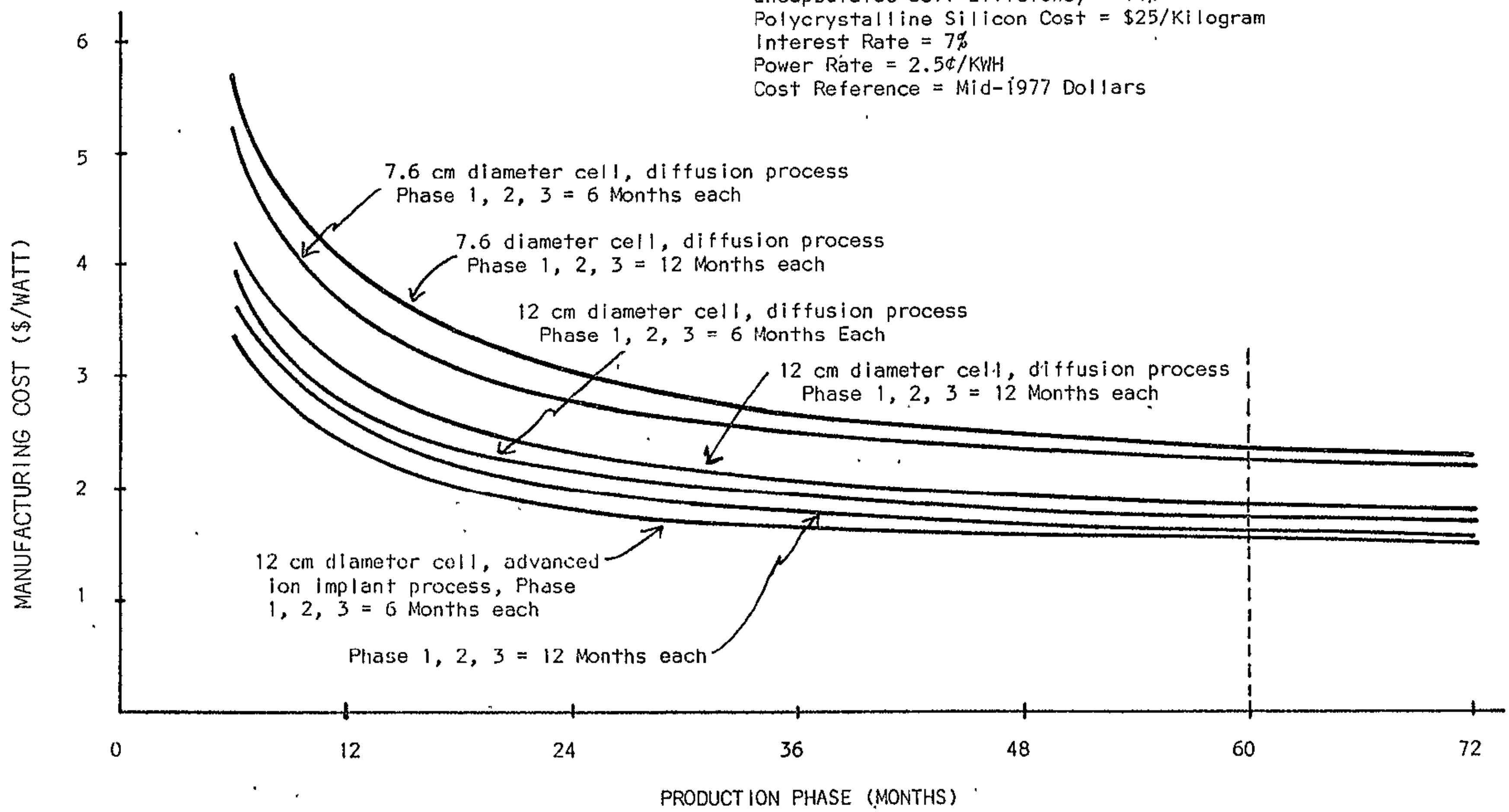


FIGURE 16. EFFECT OF THE PRODUCTION PHASE DURATION OF MANUFACTURING COST

Annual Production Volume = 25 Megawatts
Encapsulated Cell Efficiency = 14%
Polycrystalline Silicon Cost = $25/Kilogram
Interest Rate = 7%
Power Rate = 2.5¢/KWH
Cost Reference = Mid-1977 Dollars



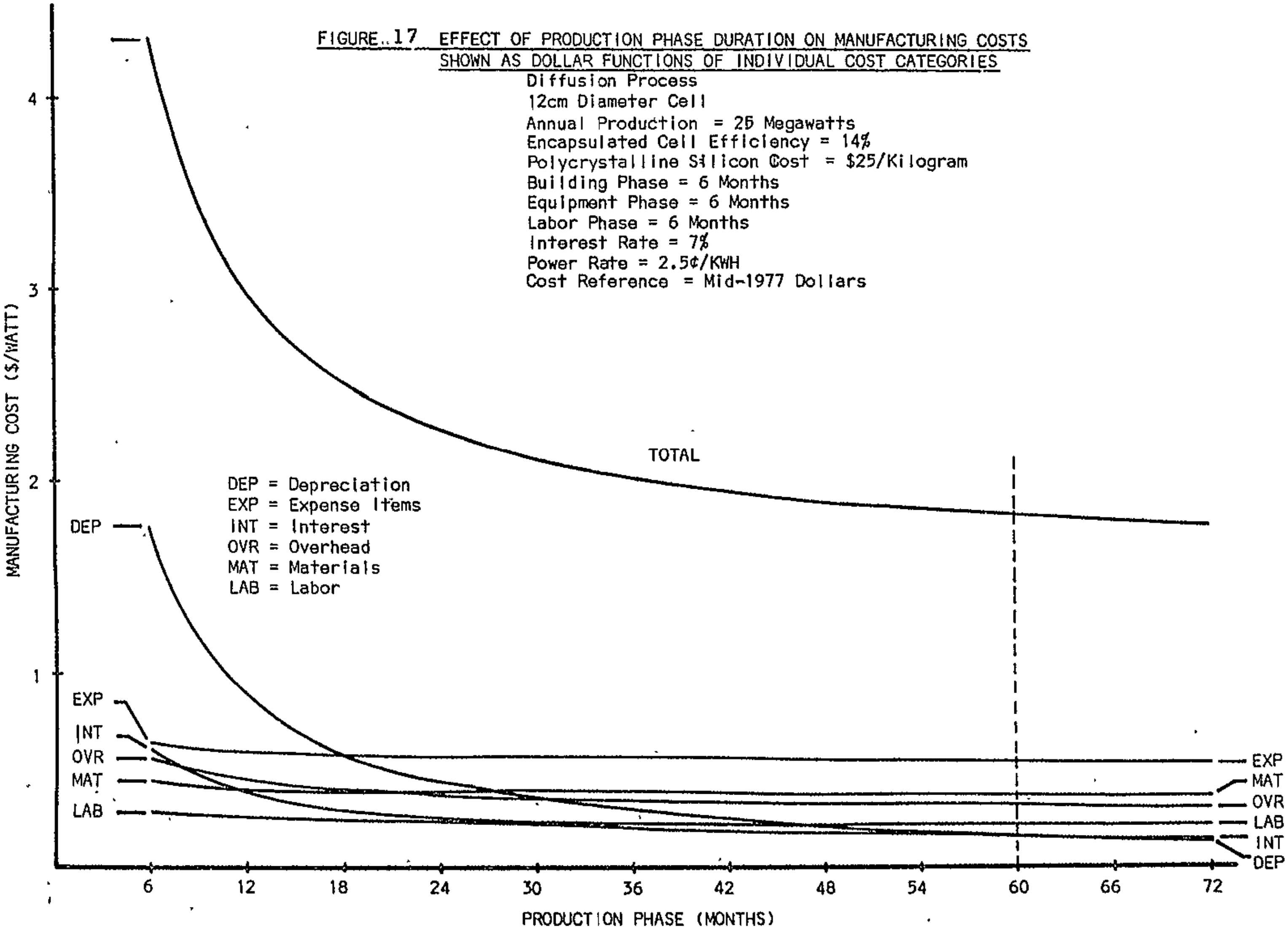
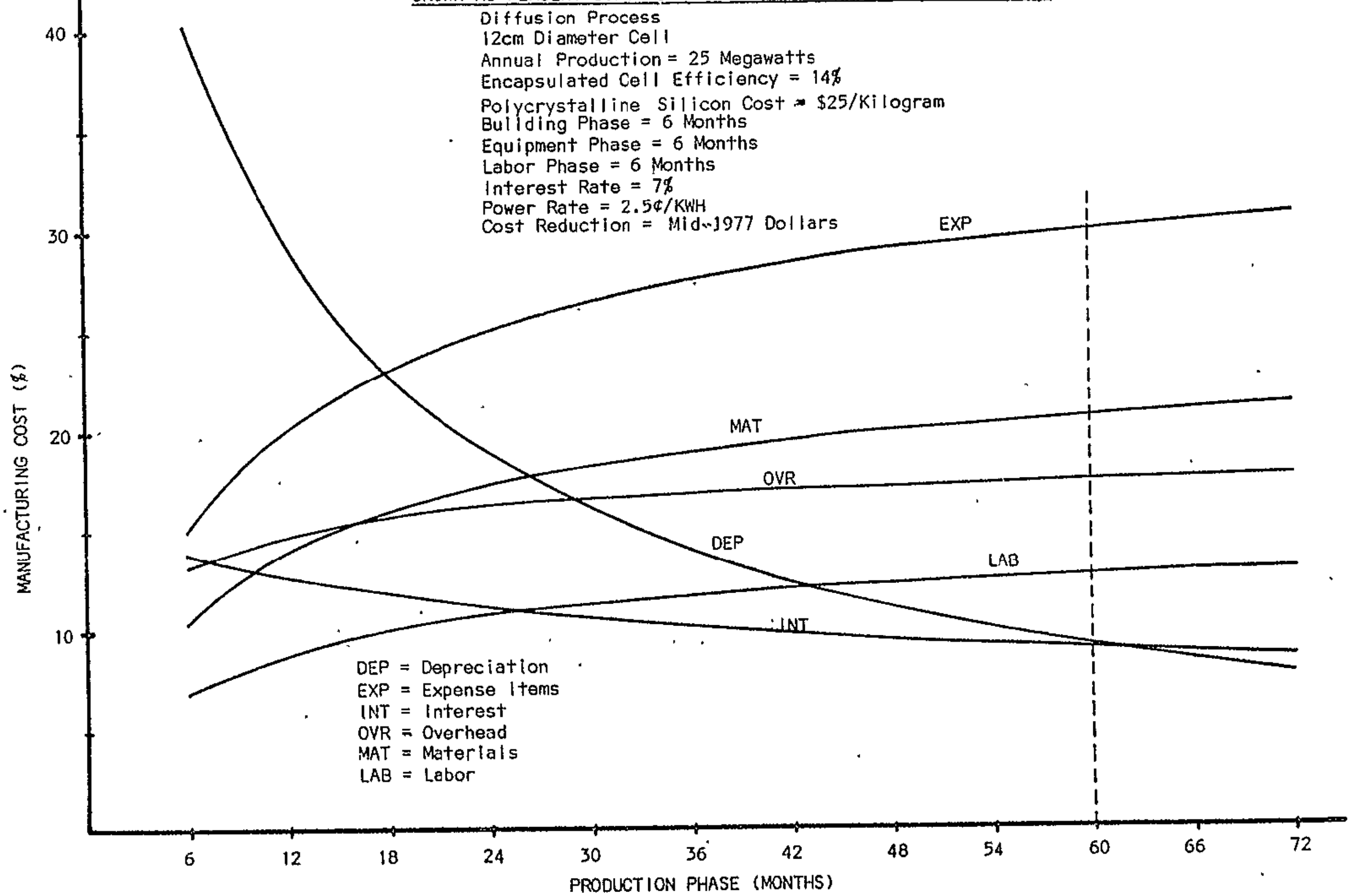


FIGURE 17 EFFECT OF PRODUCTION PHASE DURATION ON MANUFACTURING COSTS SHOWN AS DOLLAR FUNCTIONS OF INDIVIDUAL COST CATEGORIES

FIGURE 18: EFFECT OF PRODUCTION PHASE DURATION ON MANUFACTURING COSTS SHOWN AS PERCENT CONTRIBUTIONS OF INDIVIDUAL COST CATEGORIES



the factory life. Also, consumed materials, reflected as expense and materials items, predominate for long factory lives.

Two major effects of factory life associated with depreciation and total costs become apparent. The first deals with salvage value of the equipment, and the second involves introduction of advanced manufacturing technologies.

4.6.7.1 SALVAGE VALUE OF EQUIPMENT

The argument has been presented in numerous forums that outmoded equipment from solar cell manufacturing can be absorbed at a reasonable salvage value into the existing semiconductor industry. While this may be factual at very low solar cell production volumes, it is fallacious at reasonable solar cell volumes.

As will be presented in Section 4.7, the major equipment capital investment is in the crystal growth area. Absorption of crystal pullers of the size assumed in this study (the so called "olympic class" size) must occur into the silicon semiconductor industry.

An evaluation of the marketability of this equipment in the 1978 - 1985 time frame shows, that at best, limited resale can be achieved. Specifically, crystal pullers in the "olympic class", ($\geq$ 20 Kg melt capacity) that have an original value of $125K each represent nearly 50% of the initial capital equipment investment and greater than 4% of the total manufacturing cost. For an annual manufacturing volume of 25 MW, about 80 such crystal pullers are necessary. This quantity of crystal pullers represents approximately 40% of the estimated number (200) of large pullers currently existing in the world. It is further found that of the 200 units now in existance, utilization may currently be something less than 50%. Smaller capacity pullers are now rapidly becoming obsolete, saturating a resale market. The semiconductor manufacturing market could not be expected to absorb the quantity of crystal pullers estimated here.

It is, therefore, concluded that the total depreciation of equipment within the factory life is a reasonable requirement.

4.6.7.2 OBSOLESCENCE BY NEW TECHNOLOGY INTRODUCTIONS

Cost projections for solar cell modules show an anticipated price (in 1975 dollars) of \$2.00/watt in 1982, \$1.50/watt in 1983, \$1.00/watt in 1984, and \$0.50/watt by 1986. It is assumed that this price reduction will be achieved through major technology advances which will reduce the costs of polycrystalline silicon, single crystal silicon substrates, solar cell processing, and encapsulation. Further, it is assumed that these technology advances will be so significant that present technology will, in essence, be obsoleted.

The more optimistic date presented in previous sections show manufacturing costs with present technology and large volumes to reach nearly \$1.50/watt. Little or no further reductions can be expected beyond that point, and even that point may not be achievable with present technology.

A manufacturer deciding to build a factory which utilizes present technology (a necessary factor if the factory is to be operative in 1982) to achieve a selling price near \$2.00/watt faces extreme risks. If the price goal of \$1.50/watt for 1983 or \$1.00/watt for 1984 is realized by a competing advanced technology, and if the manufacturer's cost in his 1982, \$2.00/watt factory is above \$1.50/watt, he cannot compete in the market in 1983, and must close or lose money. The factory life, then, is essentially one year. Observing the data in Figure 16, the manufacturer cannot achieve a cost of \$2.00/watt with a one year factory life. A further restraint exists. If the total available market in 1982 is 25 megawatts, no one manufacturer is likely to control much more than 5 to 10 megawatts of that market. Refering back to Figure 13 for manufacturing costs at 5 to 10 megawatts annual production and combining that information with the data in Figure 16, an

even higher manufacturing cost results. The obvious conclusion is not to build the factory.

Several alternatives exist to this argument, but risks must be assumed by some group in any case.

The first option is to build the factory as soon as possible such that product manufactured at a $2.00/watt cost can be sold at a premium in 1980 and 1981, lengthening production life and increasing profitability using today's technology. Alternatively, the manufacturer may forward contract his production for 1983 and 1984 at $2.00/watt to a customer who doubts the availability of cheaper modules in that time-frame. In either case, sufficient market must exist to purchase his entire production. (It must be further assumed that a sufficiently sized market will exist only if the price is low enough to support it!)

Another alternative is merely to wait until the technology advances occur, and implement them in the factory which drives the $2.00/watt factory out of business. In doing so, the manufacturer must assume that he can capture sufficient market share with his new technology and low price that he is not excluded from entering the market at that late date, risking his business on a sudden volume jump rather than on a continuously increasing volume.

Still another alternative is that the advanced technology will not be timely. If advances are sufficiently slowed, by 2 years, for example, the factory could be justified economically. On the contrary, however, if technology advances were accelerated, it is already too late to build the $2.00/watt factory.

If a major portion of the costs could be eliminated, the factory could be built. From this study, the most effectively reduced major costs are those associated with capital equipment. If such equipment were provided, or if a market could be found to absorb it cost-effectively at the end of a short factory life, the factory could be built and run profitably.

4.7 DISTRIBUTION OF MANUFACTURING COSTS BETWEEN PROCESS AREA GROUPINGS

The manufacturing process sequence for fabrication of solar cell modules can be conveniently considered to be composed of three process sub-sequences: silicon wafer (or sheet) formation, cell manufacturing, and module fabrication (including interconnection and encapsulation). For the defined nominal values of all variable parameters, a cost breakdown has been made (for each of the cost categories) between these three process sub-sequences. Data are presented in Tables 67 through 70. Table 67 shows calculated dollar costs for each category by sub-sequence. Table 68 shows these calculated dollars as a percentage of the total cost. Table 69 shows the percentage by individual cost category totals of each sub-sequence. Table 70 presents the percentage costs by cost category within each process sub-sequence. While many observations can be made, several of them are striking. First, the single largest cost item involves expenses incurred in wafer fabrication. This is primarily a result of silicon wasted from crystal cropping and wafer sawing. Major cost reductions can be envisioned with a direct sheet growth process. Second, the largest capital contribution (seen as a function of depreciation) is again in the wafer fabrication area. Third, automation of cell processing is a fruitful cost reduction measure. Finally, reduced encapsulation requirements for cells will dramatically reduce encapsulation materials costs.

4.8 A SAMPLE FACTORY LAYOUT: 5 MEGAWATT ANNUAL PRODUCTION

The factory layout shown in Figures 19 and 20 represents the equipment facilitization, and area necessary to fabricate 5 megawatts of silicon solar cell modules annually. For this illustration, 12 cm diameter cells and a diffusion process are selected. All other variables are the "nominal" values used throughout this report. This facility was selected for illustration

TABLE 67: Cost, in dollars, in each cost category for wafer preparation, cell fabrication, and module fabrication. Costs are for a 12 cm diameter cell manufactured by a diffusion process. All variable parameters are at the defined nominal values.

COST CATEGORY		WAFER	CELL	MODULE	TOTAL
Material	K$	12166	7962	29327	49455
Expense	K$	63613	9192	145	72950
Labor	K$	6910	21945	2303	31158
Overhead	K$	24699	15216	3190	43105
Interest	K$	3680	3848	918	8446
Depreciation	K$	11912	7354	2796	22016
TOTAL	K$	122980	65517	38679	227076

TABLE 68: Costs from Table 67 as a percent of the total cost for each cost category and process sub-sequence.

		WAFER	CELL	MODULE	TOTAL
Material	%	5.4	3.5	12.9	21.8
Expense	%	28.0	4.0	0.1	32.1
Labor	%	3.0	9.7	1.0	13.7
Overhead	%	11.0	6.7	1.4	19.1
Interest	%	1.6	1.7	0.4	3.7
Depreciation	%	5.2	3.2	1.2	9.6
TOTAL	%	54.2	28.8	17.0	100.0

TABLE 69: Costs from Table 67 as a percent of each cost category.

		WAFER	CELL	MODULE	TOTAL
Material	%	24.6	16.1	59.3	100
Expense	%	87.2	12.6	0.2	100
Labor	%	22.2	70.4	7.4	100
Overhead	%	57.3	35.3	7.4	100
Interest	%	43.6	45.6	10.8	100
Depreciation	%	54.0	33.3	12.7	100

TABLE 70 : Costs from Table 67 as a percent of each process sub-sequence.

		WAFER	CELL	MODULE
Material	%	9.9	12.2	75.8
Expense	%	51.7	14.0	0.4
Labor	%	5.6	33.5	6.0
Overhead	%	20.1	23.2	8.2
Interest	%	3.0	5.9	2.4
Depreciation	%	9.7	11.2	7.2
TOTAL		100.0	100.0	100.0

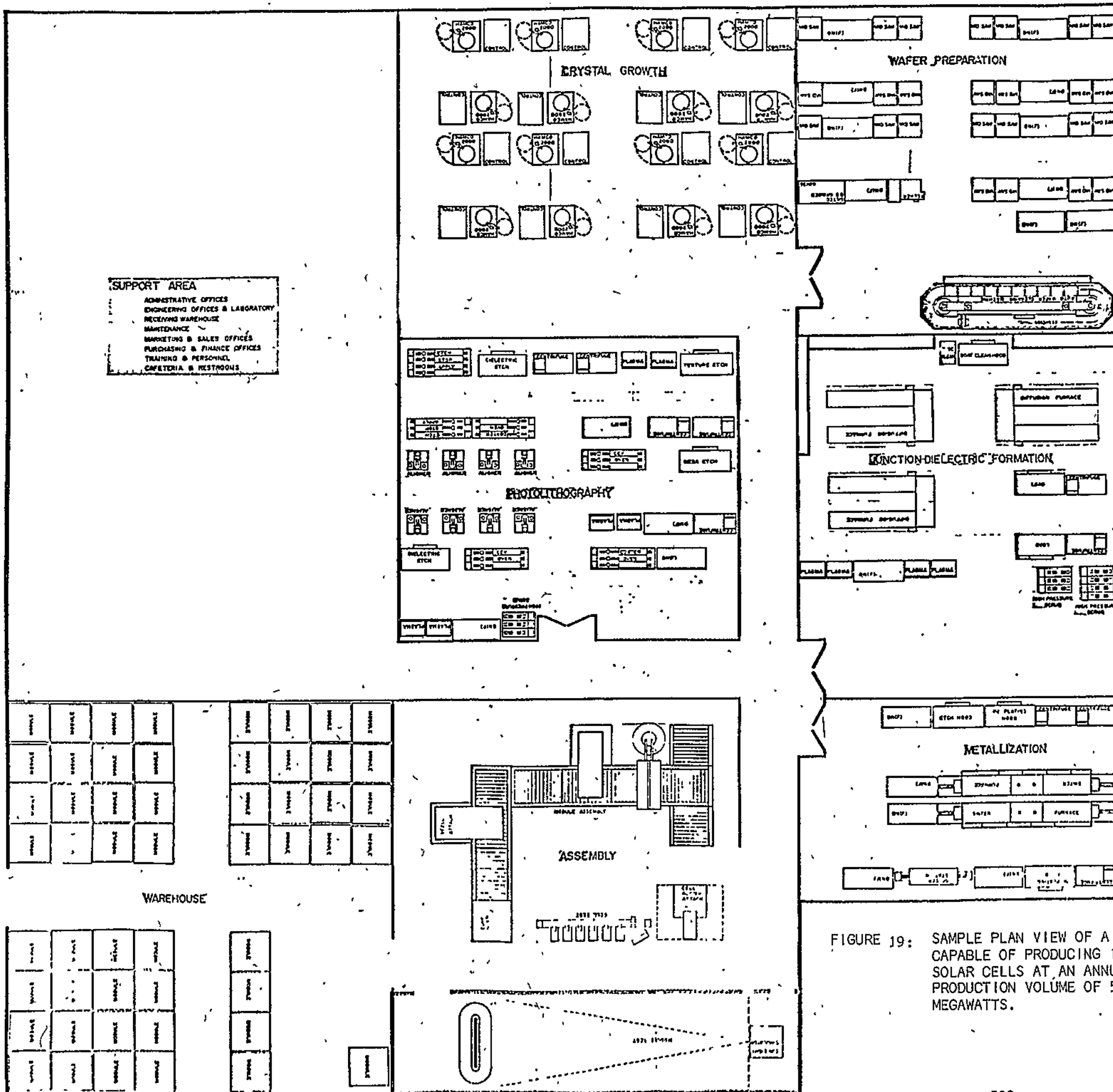


FIGURE 19: SAMPLE PLAN VIEW OF A FACTORY CAPABLE OF PRODUCING 12 cm SOLAR CELLS AT AN ANNUAL PRODUCTION VOLUME OF 5 MEGAWATTS.

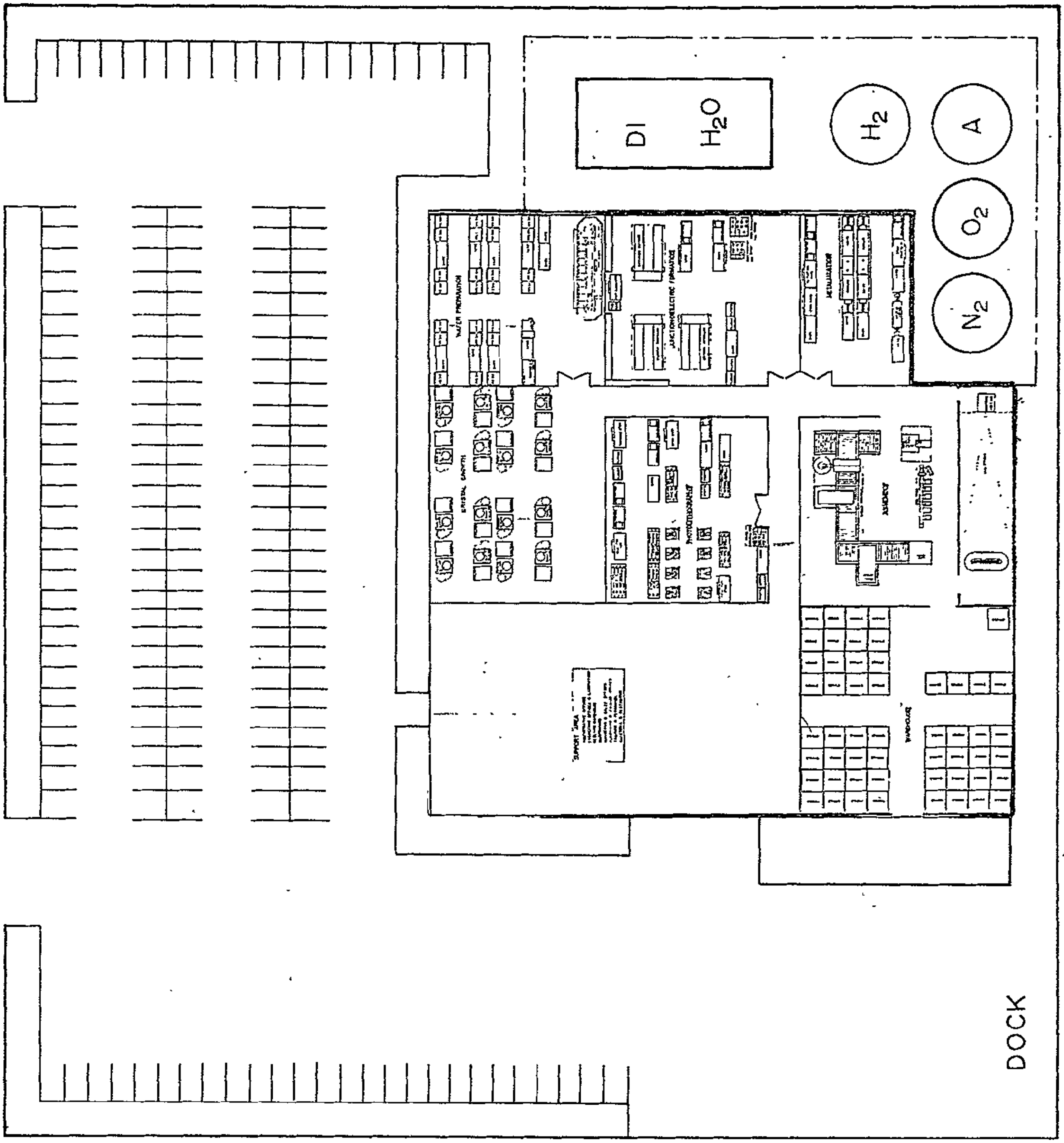


FIGURE 20: FACILITY LAYOUT, INCLUDING PARKING AND SUPPORT FACILITIES, OF SAMPLE 5 MEGAWATT ANNUAL PRODUCTION FACTORY.

purposes to show the size of a factory that would probably be necessary based on potential market size and the probable market share of any given manufacturer.

In the crystal growth area, sixteen large volume Czochralski crystal pullers are shown. These crystal pullers are 98.4% utilized and the area requires six direct labor personnel per shift.

The wafer preparation area contains all crystal sawing and etching operations. It is from this area that all solar cell material is prepared.

The three silicon solar cell processing areas (junction formation, photolithography, and metallization) are located contiguous to each other in order to establish an efficient material flow between the several processing steps. In each area, the machinery used, its utilization, and labor requirements are determined for maximum cost effectiveness.

Testing of finished silicon solar cells, assembly of these cells into modules, and subsequent testing of modules is located in the assembly area. The output from this area feeds directly into a shipping warehouse which is designed to accommodate a one month manufacturing volume.

The remainder of the factory, which is not shown in detail, is intended for all manufacturing support functions. Required industrial services are shown on the corner of the building in close proximity to all of the required usage points.

For this example, a total of 111 direct labor personnel and 93 indirect personnel are required. Parking and other related facilities are designed for this number of people.

5.0 CONCLUSIONS

A number of significant conclusions may be drawn from these studies.

5.1 ANALYSIS OF VARIABLES

A solar cell model has been described, and solar cell variables defined as operational and/or diagnostic. These variables have been identified and listed. Solar cell dimensions (size) have been identified as primary solar cell variables having the greatest impact on performance, and yet a quantitative analysis of this interrelationship has never been undertaken. Accordingly, a quantitative technical and economic analysis has been presented to identify the maximum cost effective size of a solar cell. This analysis indicated that the optimum narrow dimension of a solar cell will be near (or smaller than) 10 cm.

Five process sequences have been identified as potentially satisfying the long range ERDA goals. A list of process steps, combining the steps of the five process sequences, is presented. The primary process operational and diagnostic variables for each process step are then identified.

The primary process variables are related, in a matrix, to the primary solar cell variables. The interrelations between variables are broad and complex, demanding control of many far-reaching effects to ensure overall successful process sequence operation.

5.2 EVALUATION OF VARIABLES

Several general conclusions have been reached. First, selection of evaluation techniques has been established for the primary process variables. Second, interpretation and correlation of process variable evaluations is extremely dependent upon the process sequence chosen and must be performed

for each specific case. Finally, adequate control ranges are capable of being determined for process steps within a given process sequence. The establishment of these control ranges is an iterative process for each process sequence and cell design.

As a result of this work, it is apparent that no study can possibly establish a thorough quantitative description of process variables and their interactions. The task is enormous, and much of the information does not exist or is not published. Rather, the formalized categorization that has resulted from this program can assist in the establishment of 1) meaningful set of primary process variables (operational and diagnostic) for a particular process sequence, 2) the relationships between process variables and solar cell variables, and 3) definition of evaluation techniques for production control. In this way, the necessary continued advances in solar module production should be made possible with a minimum of wasted time, effort and material.

5.3 COST ANALYSIS

5.3.1 CELL EFFICIENCY

Future solar cell modules must have high conversion efficiency to be cost effective; the higher the efficiency the better. Solar cells with less than 13% to 14% encapsulated efficiency are unlikely to meet a $2.00/watt selling price goal if Czochralski crystal growth, sawing, and high quality encapsulation are required. At the defined nominal values of the variable parameters, a cell efficiency of greater than 13% is required. At lower production volumes or in factories with useful lives less than five years, a still greater cell efficiency would be required. Processes for either

wafer production or cell fabrication which result in lower cell efficiencies are unsuitable for future goals.

5.3.2 INCREASED ELECTRICAL POWER COSTS

As electrical power costs escalate in the future, the effect on the manufacturing cost of solar cells is relatively small. This leads to the conslusion that as alternative energy sources increase in price, solar cell energy production becomes increasingly cost effective and attractive.

5.3.3 COST INFLUENCES OF THE BUSINESS CYCLE

The manufacturing cost of solar cell modules is relatively insensitive to the interest rate on borrowed money. Accordingly, manufacturing costs for solar cell modules will be stable in the normal business cycle of fluctuating interest rates.

5.3.4 RISKS FOR THE 1982 - $2.00/WATT GOAL

The risks, without additional incentives, are too great for a manufacturer to build a factory utilizing available technology to meet a $2.00/watt goal in 1982. Technology advances can readily obsolete such a factory before it can be run long enough to be profitable. Due to competition, it is probable that no single manufacturer will have a market share of greater than 5 to 10 megawatts in a total market near 25 megawatts in 1982. This volume is marginal in effecting sufficient efficiency of operation to meet the $2.00/watt goal.

One (or both) of two courses is open to achieve the $2.00/watt goal at volume. First, forward contracting of several years production at $2.00/watt can be considered. Second, capital equipment costs can be significantly

reduced. In either case, the government is the only probable source of such funding. Without such funding, it is questionable whether or not \$2.00/watt can be achieved in 1982.

5.3.5 RESEARCH AND DEVELOPMENT FUNDING

Several areas of technology advancement would be especially fruitful in reducing costs. Significant savings can be achieved if capital and expense costs can be reduced in the crystal growth and sawing areas. The cost of polycrystalline silicon should be minimized, but, by itself, is not sufficient to reduce costs to very long range goals. The crystal growth and sawing capital costs could be reduced if there is developed by that time an effective direct silicon sheet growth technology (which will, later, permit ultimate goals to be achieved). Other fruitful areas include automation of processing to reduce labor contributions to costs, and minimization of encapsulation requirements to lower costs of materials consumed.

6.0 APPENDIX: DESIGN AND PROCESS INTERACTIONS

6.1 DESIGN IMPROVEMENTS

In order to effectively evaluate processes and process sequences, it was first necessary to establish minimum, or baseline, design considerations for the solar cell and its constituent elements. It has been Motorola's contention throughout this contract that it is necessary to develop a solar cell design model (or design models) which effectively characterize the highest efficiency silicon solar cell capable of being produced utilizing current or anticipated semiconductor processing techniques, subject to the major constraint that the estimated cost in dollars per watt of the final assembled and installed array of silicon solar cells be minimized. Any process sequence, thus, must be based on a solar cell design model which reflects current state-of-the-art practices as well as additional concepts not currently incorporated in solar cells but envisioned as likely to contribute to future solar cell improvement. The following sections first treat basic design considerations, and then discuss specific solar cell design features.

6.1.1 BASELINE DESIGN MODEL CONSIDERATIONS

A solar cell can be considered as a co-operative group of individual elements, including an antireflection coating, the front surface, a junction region, a substrate, a back surface, and front and back metallizations. Each element can be characterized with a list of desirable properties.

6.1.1.1 ANTIREFLECTION COATING

Desirable features of an antireflection coating on a solar cell include those which:

(i) optimize the transmission of incident photons into the silicon material;

(ii) promote the lowest concentration of surface-state recombination centers at the coating-silicon interface;

(iii) aid in establishing an electric field within the silicon (near the surface) which retards minority carrier flow toward the front surface and recombination at the front surface; and

(iv) passivate and isolate the P-N junction perimeter.

6.1.1.2 FRONT SURFACE

The silicon solar cell should possess a silicon front surface condition which:

(i) minimizes surface defects and maximizes minority carrier lifetime near the silicon surface;

(ii) minimizes surface recombination velocities;

(iii) maximizes the absorption of incident photons by the silicon, complementing the antireflection coating;

(iv) refracts the incident light to optically enhance the possible photon path lengths through the silicon substrate;

(v) promotes the adhesion of metal ohmic contacts.

The surface may be that of an as-grown sheet of silicon, or it may be polished or etched. When the orientation allows, as discussed Section 6.1.2, texture etching can provide a highly controllable, cost-effective way of obtaining most of the properties listed above while accruing additional benefits for solar cell design. A model for a textured front surface is discussed in further detail in Section 6.1.2 of this report.

6.1.1.3 JUNCTION REGION

We consider in our baseline design model only the case of the

silicon P-N junction solar cell, which must have a thin, front surface region with an electrical conductivity opposite that of the substrate (e.g., N type surface region on a P type substrate) which:

(i) forms a metallurgical P-N junction;

(ii) is amenable to formation of an ohmic contact without significant degradation of solar cell performance;

(iii) has a low surface recombination velocity, or is designed to effectively minimize surface recombination effects (e.g., has a large built-in drift field);

(iv) has sufficiently high minority carrier lifetime;

(v) has a sufficiently low value of sheet resistance; and

(vi) maximizes the collection efficiency for short wavelength photons.

Property (vi) implies that the P-N junction depth below the front surface be as shallow as can be allowed, subject to satisfying the other five requirements. Traditionally, only junction depths of about 0.5 micron or less have been used, and the best (violet-type) cells have junction depths closer to 0.1 micron. This requirement makes attainment of property (v) more difficult.

6.1.1.4 SUBSTRATE

The solar cell must have a silicon substrate which:

(i) has high minority carrier lifetime for a maximum photo-current generation;

(ii) has a sufficiently high impurity doping level to obtain high open circuit voltage and low electrical resistance;

(iii) is optically thick enough to efficiently absorb an appreciable fraction of incident long wavelength photons but is mechanically

thin enough to conserve silicon; and

(iv) has a low minority carrier recombination velocity at the back surface, or is designed to have a large drift field to effectively minimize back surface recombination effects.

Minority carrier lifetime is of extreme importance to efficient silicon solar cell performance; however, lifetime values practically obtainable may eventually be dictated by economical silicon purification processes. Under more immediate control, and of particular interest insofar as a design model is concerned, is the optical thickness of the silicon substrate. The optical thickness may be enhanced (for a given mechanical thickness) by forcing absorption paths to be other than perpendicular to the cell plane (or P-N junction), and additionally through multiple internal reflections.

6.1.1.5 BACK SURFACE

The solar cell should have a silicon back surface condition which:

(i) minimizes surface defects and maximizes minority carrier lifetime near the silicon surface;

(ii) minimizes surface recombination velocity; and

(iii) reflects unabsorbed incident radiation which passes through the substrate and reaches the back surface.

By reflecting photons reaching the back surface, the optical thickness of the substrate can be at least twice as great as the physical thickness. Moreover, unusable infrared wavelength photons can be re-radiated from the front of the solar cell rather than absorbed at (or near) the back surface.

6.1.1.6 METALLIZATIONS

The solar cell must have metallization contacts to both front and back surfaces which:

(i) provide ohmic electrical contact to the opposite sides of the P-N junction;

(ii) allow reliable, low-loss interconnection with other solar cells and with external circuits;

(iii) minimize solar cell internal series resistance;

(iv) cover (and therefore shadow) a minimum of the cell front surface area;

(v) allow optical reflection from as large a fraction as possible of the back surface area; and

(vi) are corrosion resistant.

6.1.2 TEXTURED SURFACE

A textured surface, consisting of a uniform distribution of minute pyramids as shown schematically in Figure 21, causes light reflected from the first impingement on the solar cell surface to strike the solar cell at least a second time (assuming initial normal incidence). This second impingement increases the amount of light absorbed in the solar cell, improving cell efficiency by reducing the total amount of light reflected from the cell. Incoming, reflected, and refracted ray traces of light normally incident to the overall solar cell, Figure 22, show the multiple reflection features of this surface topography.

Another major effect of front surface texturing is that, since light is refracted into the silicon at an angle to the normal of the overall solar cell plane, more light is absorbed within a given thickness of silicon than would occur with normally incident sunlight on a smooth-surfaced solar cell. This

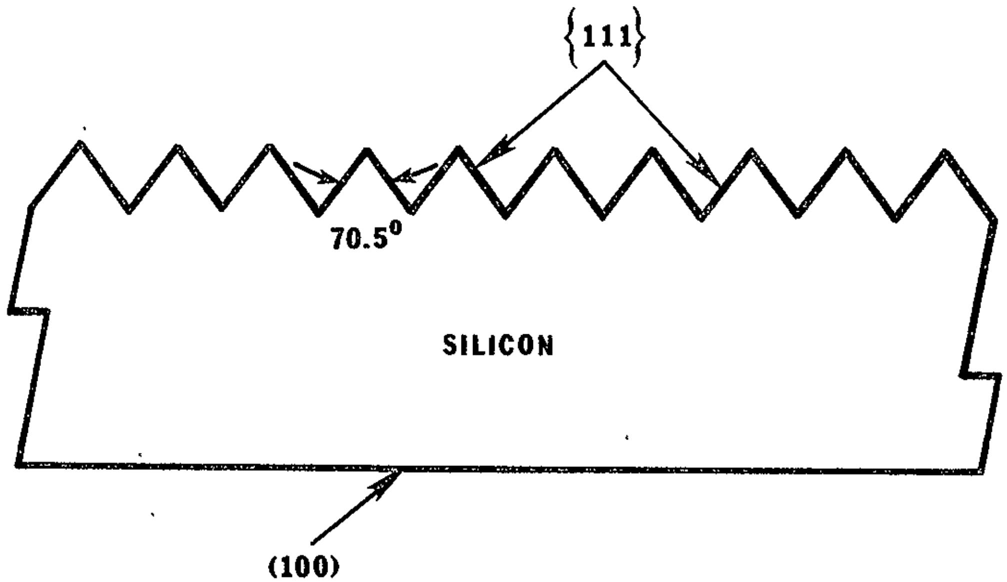


FIGURE 21: Cross-sectional diagram of silicon (100) wafer showing geometry of textured surface having {111} faceted pyramids.

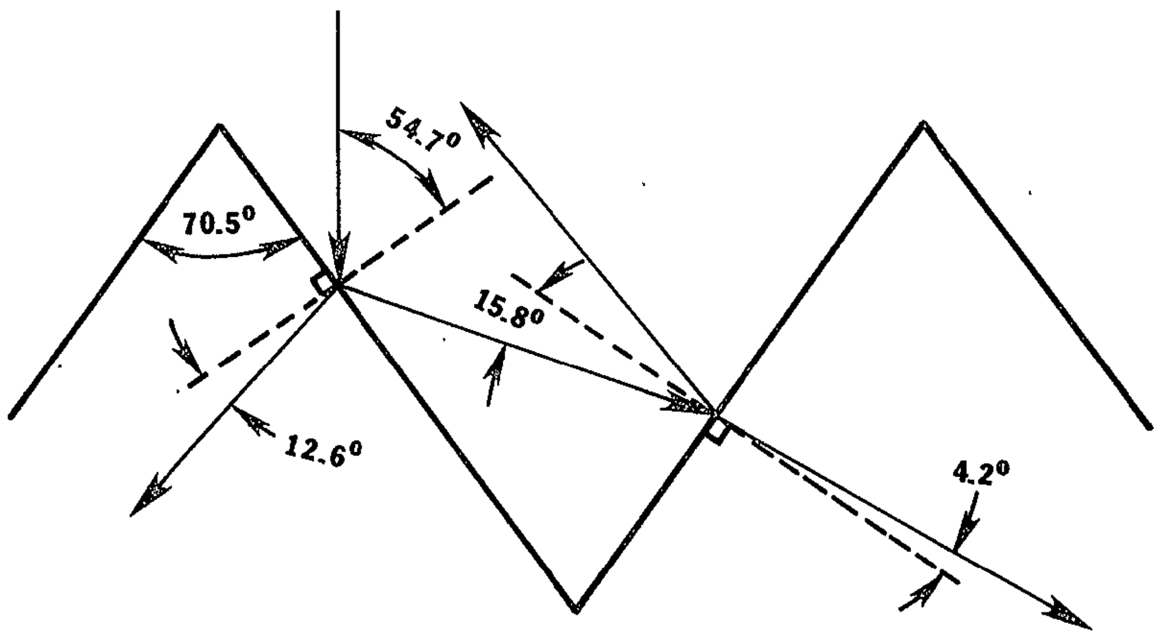


FIGURE 22: Diagram of reflected and refracted ray traces and angular relations for light normally incident to the substrate (100) plane of a textured surface solar cell.

property can be separated into its effects in two regions: a microscopic region involving the volumes immediately adjacent to the p-n junction, and a more macroscopic region involving the bulk of the silicon below the junction.

In the microscopic region near the junction, it is first assumed that the surface relief of the pyramidal structures is large (averaging greater than 10μ) compared to the p-n junction depth (less than 0.5μ). Light normally incident to a textured surface solar cell strikes the surface facets at an angle near 55°. Figure 23 diagrammatically demonstrates the refracted paths of a normal incidence light beam on a smooth surface cell and also in an analogous fashion on a textured surface facet. The optical path length of the refracted beam within the region of the junction is greater than the normal path length by a factor of $\frac{1}{\cos\phi}$ in the case of the textured surface. This increased path length has an effect equivalent to increasing the absorption coefficient of light in the silicon by the same factor (over the smooth cell normal incidence beam). Thus, within the region near the junction, more light is absorbed, creating more carriers, and increasing cell efficiency for very shallow junctions. Assuming that the index of refraction of silicon is 3.75, the angle ϕ is approximately 12.6° and $\frac{1}{\cos\phi}$ is approximately 1.025. While this near surface (microscopic) phenomenon is effective throughout the solar spectrum, it is most significant in the short wavelength end of the solar spectrum where the silicon absorption coefficient is greatest. The phenomenon is, thus, expected to enhance somewhat the blue response of the solar cell.

A larger effect is seen in the macroscopic region within the bulk of the cell below the microscopic junction region. Light incident normal to the plane of the overall cell is refracted by the textured surface through an angle of 12.6° from the normal to the facet. (Figure 22). This is equivalent to an angle of 42.2° from the normal of the overall cell, i.e., ϕ=42.2°, Figure 23, so that the path length through the bulk is increased

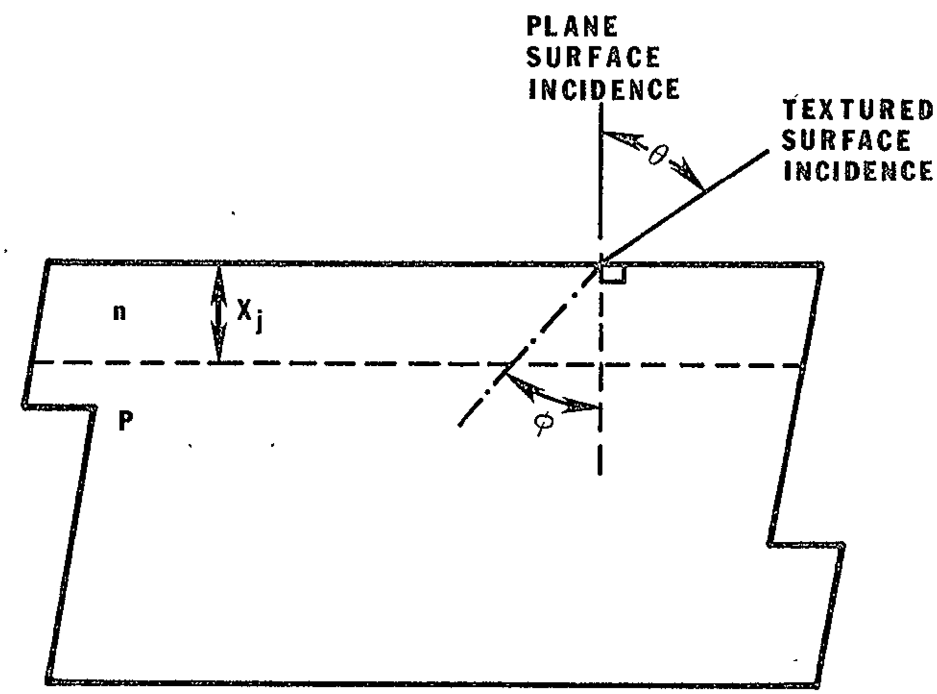


FIGURE 23: Representation of increased absorption path length of textured surface light ray trace compared to trace normal to a plane surface.

by a factor of $\frac{1}{\cos 42.2°}$, equal to 1.35. This is the equivalent of increasing the path length through the bulk by 35%, making each three units of solar cell thickness look like four units of thickness. Restated, the number of carriers created in an optical path length of four thickness units is generated within three mechanical thickness units of the front surface and the p-n junction. This makes the cell far more responsive to the longer wavelengths of incident sunlight, which have smaller absorption coefficients in silicon than the short wavelengths.

A further effect of the angle of travel of the refracted beam through the bulk occurs at the back surface of the cell. If the back surface of the cell is not textured and is a plane, all light refracted through the front textured surface can be shown to strike the back surface of the cell at an angle exceeding a critical angle, resulting in total reflection from the back surface toward the front surface. (The condition for total internal reflection

$$n_{Si} \sin \varepsilon = n_{ext}$$

yields angles of about 15.5° for air and near 24° for most plastics and SiO_2.) Total internal reflection occurs when the angle ϕ exceeds the angle ε, Figure 24. The angle ϕ for normal incidence on the textured front surface is 42.2°, thus satisfying the condition for total internal reflection. Non-normal incidence will produce different values for the angle ϕ, but the angle ϕ will always satisfy total internal reflection conditions.

Total internal reflection from the back surface can be advantageously utilized in one of two ways. First, the internally reflected beam will be further absorbed on its second pass through the material, again creating more carriers and increasing cell efficiency. Alternately, a thinner cell (conserving silicon) could be made to display the same efficiency as a thicker standard cell. The magnitude of the effect of the second pass absorption will be, of

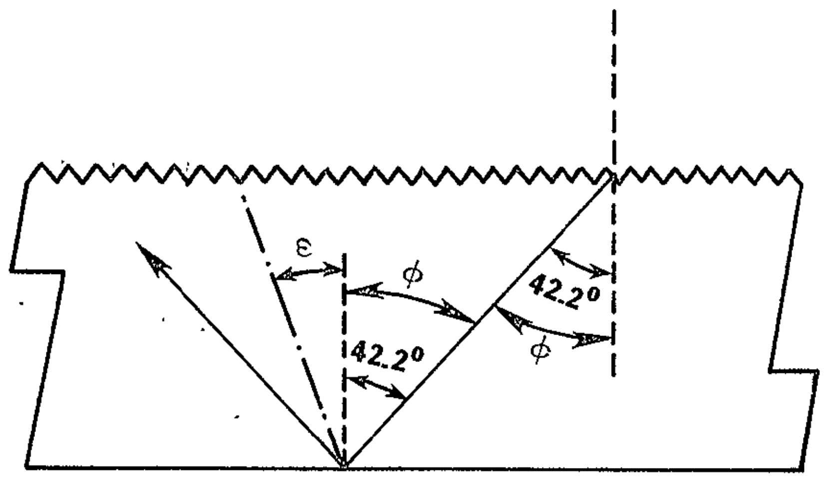


FIGURE 24: Path of beam refracted from textured surface illustrating total internal reflection from back surface if the brewster angle ε < 42.2°.

course, a function of the total cell thickness and the minority carrier lifetime of the cell substrate.

More subtle advantages also occur with a textured surface. The textured surface, formed by etching, leaves a surface which is relatively free of work damage. A plane surface, on the other hand is often achieved by polishing, leaving a finite degree of work damage in the crystal surface layer. Such damage is known to adversely affect both carrier lifetimes and surface recombination velocity; it can propagate during high temperature processing, aggravating the damage. This additional advantage of textured surface etching will not apply to solar cells fabricated from silicon ribbon (if it is directly grown to have smooth, damage-free surfaces), or from chem-etched wafers.

For any unit area in the plane of the substrate, the (100) plane, the corresponding area of the textured surface described above will be a factor of $\sqrt{3}$ times larger. When ohmic metal contacts are applied, this increased surface area will serve to reduce the magnitude of the contact resistance. Furthermore, the textured surface itself can promote better metal adhesion to the silicon surface.

Finally, the mechanism causing reduced reflection of incident light discussed at the outset of this section will also lessen the requirements on antireflection coatings chosen for the solar cell surface. For example, the differences in total reflection obtained when using a perfectly matched antireflection coating and when using a somewhat less than perfect one will be much less pronounced, perhaps allowing coatings to be chosen for increased cost-effectiveness and convenience of processing.

6.1.3 FRONT SURFACE METALLIZATION

Metal coverage and series resistance tradeoffs are major limiting design considerations on the shape and maximum useful size of solar cells, and the concomitant material process for producing silicon sheet. A critical evaluation of existing metallization geometries has revealed that efficiency may suffer if these designs are extended to large area ribbon or sheet cells. Accordingly, improved contact metallization designs were investigated. Designs which show the greatest promise over existing designs for improved cell performance have multiple contacts; hence the interconnect and packaging systems should consider the possible need for multiple-contacts-per-wafer. Also, efficient design seems to favor long, narrow rectangular ribbons rather than large area square or round sheet solar cells.

In particular, the front surface metal pattern of a silicon solar cell will influence the performance of both solar cells and modules because of three requirements: 1) the pattern must provide area for an interface point (or points) for electrical connection to other cells; 2) the pattern must provide sufficient area for efficient (low resistance) flow of current, since the metal pattern itself (as well as the cell below) will have an internal series resistance; and 3) the pattern should shadow the least possible area to maximize current generation. Some preliminary conclusions regarding constraints on metal pattern design and on solar cell size can be drawn quickly by considering interactions of these three requirements.

Assume that a silicon solar cell is available with any desired surface area or shape but is constrained to have a fixed, minimum value of surface sheet resistance above the P-N junction. Series resistance of the cell will then depend on the thickness of metal used for a particular front ohmic contact

pattern and the resistivity of that metal. If the metal pattern coverage is limited to a reasonable percentage of the front surface area (say, 5 to 10%) and a particular metal system and thickness are adopted (defining sheet resistance), then series resistance depends on pattern topology. The metal "current collection" fingers on the cell surface may contribute appreciably to series resistance. For a single contact region solar cell, as the cell surface area becomes larger (and the metal current-conducting paths become longer) a point will be reached where series resistance has increased beyond an acceptable value. In effect, the permissible surface area of the solar cell has been limited.

This is not true if more than one external electrical contact can be made to the cell. In this case, only one lateral dimension of the solar cell surface needs to be limited. For example, a solar cell fabricated on a rectangular ribbon substrate may be infinitely long if electrical contacts are made along its edges at small intervals, but there must be a practical limit on the width of the cell if acceptably low internal voltage loss (i.e., series resistance) is to be maintained. Calculations have shown that as ribbon widths surpass 10cm, loss of efficiency increases so rapidly that such cells are no longer cost effective, Section 3.2. The same principle holds for circular solar cells. Constrained to a fixed area of front surface metal, a circular cell may require multiple contact points around the perimeter to maintain a low series resistance. A larger diameter cell would require more contacts than a smaller diameter cell; and in the limit, as cell diameter becomes still larger, overall cell efficiency must suffer.

The net effect of using multiple electrical contacts at the perimeter of a solar cell is to shift some of the burden of summing the photo-current generated by the active surface of the cell away from the metal pattern on the

cell surface to external electrical busses. When such a solar cell is assembled in an array of cells, an additional benefit accrued is increased reliability achieved through partial redundancy of the multiple cell contacts.

6.1.4 BACK SURFACE METALLIZATION

The physical configuration of the back surface of a solar cell will influence its optical properties. It is important from a design standpoint to know, as a function of wavelength, the degree of light absorption, reflection, and transmission at the cell back surface, since these factors will influence cell efficiency as a function of thickness (multiple light pass from reflection) and heating effects (absorption at the back surface).

Another variable affecting optical performance at the back surface is the configuration of the front surface. If the front surface is texture-etched and the back surface is non-absorbing, for example, total internal reflection from the back surface should always occur.

Experiments have been performed to measure, as a function of wavelength, the reflection of light from the back surface of a silicon wafer with various front surface and back surface configurations. The purpose of these experiments was to determine if any cell performance advantages can exist with a patterned back metal. Samples with both polished (or isotropically etch-polished) and texture-etched front surfaces were utilized for each back surface configuration.

Test cells were prepared from 0.8 - 1.2Ωcm p-type silicon wafers. The starting wafers were isotropically etched on one side and polished on the other. Some of the test wafers utilized the polished side as the back surface, and others used the etched side as the back surface. The front surfaces of all test wafers were prepared such that one-half of the wafer was texture-etched. The entire front surface of each test wafer was then coated with 700A of silicon nitride to serve as an antireflection coating.

Half of the back surface of each test wafer was similarly coated with 700A of silicon nitride while the other half was covered with a thick metal film. The back was configured in such a way as to divide the entire test wafer into four classes of front/back surface condition combinations:

1. textured front/dielectric back;
2. textured front/metal back;
3. smooth front/dielectric back;
4. smooth front/metal back.

Integrated sphere reflection tests were then performed. Data were taken over wavelengths from 0.35μm to 2.0μm to determine the reflectance characteristics of the interface at the test wafer back surface.

In each case where the back surface was covered with metal (which had been sintered) the empirical reflectance curves agreed perfectly with theoretical curves for reflectance from the front surface of the silicon wafers. The smooth front surface reflectance approached a value of 30% at 2.0μm, and the textured front surface reflectance approached a value of 10% at 2.0μm. In both cases where the test wafer back surface was covered with dielectric (and, during the measurements, backed by an extremely efficient absorber) a back surface reflectance effect was observed. For wavelengths below 1.1μm where the silicon wafer absorption is good, reflectance curve shapes are identical for both dielectric-covered and metal-covered back surface wafers. (The wafers utilized in these measurements were sufficiently thick to totally absorb any light in this wavelength range reflected from the back surface.) However, for wavelengths longer than 1.1μm, where silicon becomes transparent, an additional reflectance component was observed for wafers with dielectric coated backs. The smooth front surface test wafer reflectance approached 50% at 2.0μm, and the

textured front surface test wafer approached 50% reflectance at 2.0μm. Therefore, in going from a metal backed cell to a dielectric backed cell, the smooth front surface wafer shows a 33% increase in reflectance while the textured front surface wafer shows a 400% increase in reflectance. This large increase in reflectance for textured surface wafers is a result of the total internal reflection condition inherent to textured wafers.

The possibility of patterning the back surface metal in order to utilize reflection of the longer wavelength portions of the solar spectrum back toward the front surface has ramifications other than increased absorption of useful light. For example, infrared wavelengths longer than 1.2 micrometers can be reflected from the back surface and ultimately out of the module, reducing cell and module operating temperature and increasing module efficiency. Also, a cost trade-off occurs between the additional cost of patterning the back surface metal, the cost savings of decreased metal consumption, and the effective cost reduction brought about through increased cell efficiency.

6.1.5 METALLIZATION TEST PATTERN

As discussed in the two previous sections, a major factor in determining solar cell performance is the metallization pattern. The metallization must efficiently collect current while shadowing the minimum active area. In achieving optimum designs, thus, it is necessary to determine allowable contact metallization line widths, both from an achieveable fabrication feasibility standpoint and from a series resistance standpoint.

The limitations of metal contact pattern linewidths will vary with the surface flatness of the silicon. Accordingly, two types of surfaces were studied: polished and textured etched. These two types of surfaces represent extremes in surface microscopic smoothness. Both, however, are on macro-

scopically plane surfaces and will not necessarily present the effects of surface warp or ripple possible from sheet or ribbon growth. The effects of these latter parameters must be evaluated when sufficient representative ribbon samples become available.

A test pattern photoresist mask, Figure 25, was designed with linewidths ranging from 0.0003 inch to 0.0500 inch. Dielectrics (or metals) can be patterned on the desired surfaces by standard photolithographic techniques.

The evaluation technique, on both polished and textured test wafers, included the formation on the surface of a dielectric, either silicon dioxide or silicon nitride, and patterning the dielectric with the test pattern. The patterns were visually inspected and evaluated. The patterned wafers were then electroless nickel plated and solder coated. Optical inspections indicated minimum linewidth limitations due to photoresist procedures, and electrical continuity measurements determined line resistance after soldering. Sheet resistance versus metal linewidth was tabulated for both textured and polished surfaces to determine the relative ohmic properties of a small number of wide lines versus a large number of narrow lines for solar cell current-collecting patterns.

Results indicated that there is no problem in obtaining the smallest (0.0003 inch) line width on polished wafer surfaces using standard photo-lithographic techniques and equipment. To the contrary, textured surfaces present a special problem. In order to maintain the integrity of the dielectric covering the peaks of the textured surface pyramids in areas where no preohmic pattern is to appear, a much more viscous photoresist must be used, as discussed in a Section 6.1.6. Application of this viscous resist produces a much thicker layer in the "troughs" of the textured surface, and this, in combination with the optical properties of the textured surface itself,

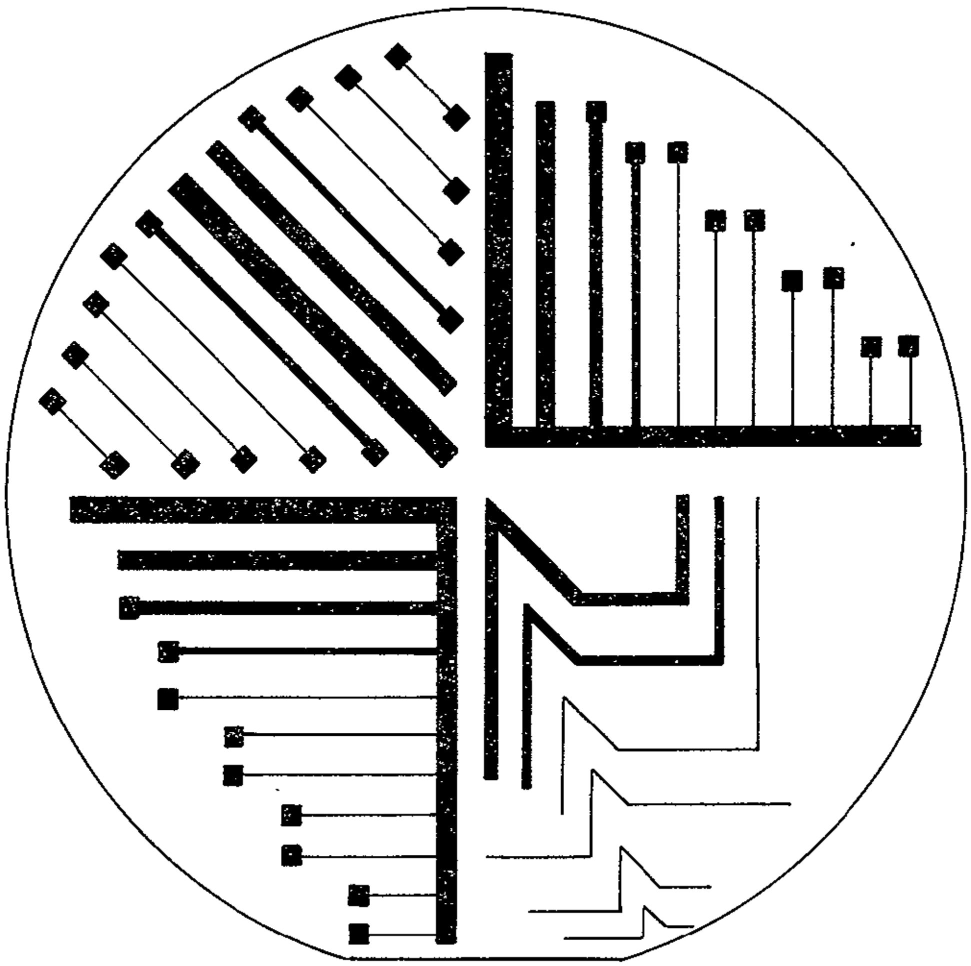


FIGURE 25: Metallization and solder test pattern. The pattern contains linewidths ranging from 0.0003 inch to 0.0500 inch. Pattern is designed such that lines are withdrawn from solder coating at horizontal, vertical, and angular directions. In addition, the pattern contains included angles of 45°, 90°, and 135°.

seems to set a practical lower limit on preohmic line width resolution. Patterns were formed by contact printing from the mask. Inspection has shown that line widths smaller than 0.001 inch have not been clearly and consistently opened. Textured surface pyramids may have base widths on the order of 10 microns; therefore linewidths of 0.0005 inch (12.7 microns) may encompass only a single pyramid. Pyramid heights on the order of 10 microns prevent true contact printing. Thus, light scattering among the pyramids contributes to an inherent limit of line width resolution. Exposing with a more collimated light source, such as is used with projection or proximity printing, should help to minimize these effects.

Wafers used for photolithographic studies, as well as a comparable set of polished test wafers, were plated with nickel and solder-dipped to obtain maximum metal build-up for a given line width. These lines were then measured for sheet conductance/resistance.

Experiments have been performed with textured surface wafers coated with silicon dioxide and prepared using standard viscosity (44 cp) photoresist to allow formation of soldered metal lines with widths between 0.0003 inch and 0.0500 inch. For line widths less than or equal to 20 mils, soldered line sheet resistance ρ (in Ω/sq.) is given by

$$\log \rho = -1.09 - 0.75 \log W,$$

where W is the line width in mils. This means ρ is proportional to $W^{-3/4}$. (If the solder bead build-up were hemicylindrical, then ρ would be proportional to W^{-1}.) For line widths greater than 20 mils the capillary effect of fine lines tends to become suppressed and the sheet resistance tends to become independent of line width, indicating a constant thickness at the larger widths.

The relation between sheet resistance and line width (given above) for lines less than 20 mils wide implies that, for a given area of metal line

coverage, one wide contact finger will introduce more series resistance than two contact fingers distributed over the same active cell area, but each finger being half as wide. Thus, for soldered contact systems of equal total area, many narrow fingers are more efficient than fewer wide fingers, as long as the thinnest lines are at least 0.001 inch wide to preserve physical and electrical continuity.

6.1.6 TEXTURED SURFACE-PHOTORESIST INTERACTIONS

Solar cell fabrication is accomplished by performing a number of individual process steps in a process sequence. While isolated individual process steps may appear satisfactory when assessed alone, experience in the semiconductor industry has shown that most process steps require modification and trade-offs when incorporated into an optimum process sequence. Such modifications may necessarily be drastic, making an otherwise seemingly desirable individual process step undesirable when utilized in the sequence.

As an example of process step interactions, a process sequencing study investigated photoresist coverage of textured surfaces. The study identified an undesirable effect, resulting in corrective modifications to the photoresist procedure.

A process interaction between photolithography of dielectrics on textured surfaces and plating of metal contacts was observed. The dielectric is deposited on the textured surface to act both as an antireflection coating and as a plating mask. Following dielectric deposition, the dielectric is patterned photolithographically to define the metal contact pattern; and the metal contacts are plated into the pattern openings. (The retained areas of dielectric serve as a plating mask.) Failure of the dielectric as a plating mask can be observed

in a scanning electron microscope (SEM) photomicrograph (5000X), Figure 26 . Here, metal has plated onto unintentionally exposed silicon peaks of the textured surface.

In our laboratory, normal photoresist procedure for polished wafers utilizes thin, 44 cp (0.044 $N \cdot S/m^2$) photoresist and spin speeds of 5000 rpm. This procedure was applied initially to patterning silicon nitride dielectric layers deposited on textured surfaces, and resulted in exposure of silicon peaks and their subsequent plating with metal. Following identification of this phenomenon as a photoresist problem, the photoresist technique has been modified. Complete photoresist protection appears to be achieved by increasing photoresist viscosity to 240 cp (0.24 $N \cdot S/m^2$) and reducing spin speeds to 3000 rpm.

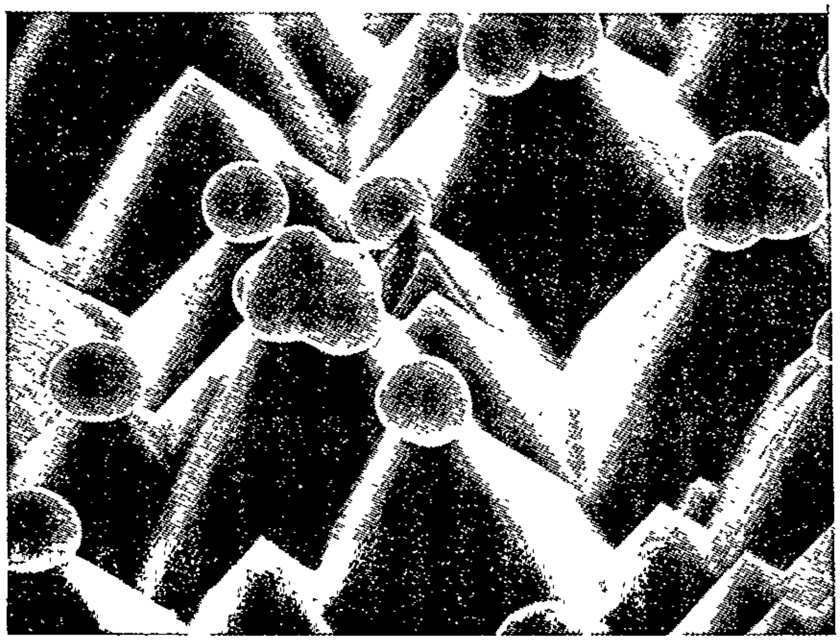


FIGURE 26: SEM Photomicrograph of electroless nickel plated surfaces of unprotected pyramid peaks, 5000X, 60° tilt.

6.1.7 SCHOTTKY BARRIER SOLAR CELLS

Silicon solar cells can be broadly classified as either Schottky barrier solar cells or P-N junction solar cells. Either, in theory, could meet the goals of the LSSA Project. In order to obtain the LSSA Project goal of silicon solar cell modules which operate with at least 10% efficiency, it is necessary that the individual cells operate at greater than 10% efficiency. This is required since module optical transmission losses, thermal resistance, cell packing density, and space utilization will lower the overall efficiency.

A survey of the recent literature on Schottky-type cells has been performed, and a list of references in chronological order appears at the end of this section. No reference has been found which reports large area silicon Schottky-type solar cells which exhibit greater than a 9.5% efficiency.[9] (Schottky-type cells with 15% efficiency have been reported on GaAs.[15]) Recent professional society conferences have given no indication that a breakthrough in the present state-of-the-art of silicon Schottky cell technology is imminent, although studies are continuing. In fact, although theoretical computations have been mentioned in the literature claiming that the upper limit on conversion efficiency is slightly better for the Schottky barrier cell than for a P-N junction cell,[7] the state of the technology is quite the opposite.

Metal-semiconductor solar cells reported to date exhibit inherently low output voltages. This effect is a consequence of high diode "saturation" (dark) currents and low metal-semiconductor barrier heights. Thus, the possible high photo-generation current densities theoretically available with Schottky cells are offset by low output voltages.

Metal-oxide-semiconductor solar cells[5,12] have been fabricated, exhibiting open circuit voltages as high as 0.52 volts.[18] In such cells, current flow

requires tunneling through the interfacial layer. The best such cells have shown only an 8% conversion efficiency,[8,16] indicating reduced current collection efficiency (through the interfacial layer) compared to the metal-semiconductor cells.

No experimental results have been shown to give credence to the possibility of obtaining increased Schottky cell voltages while maintaining high currents. On the other hand, the high generation current possibilities ascribed to such cells can be approached by P-N junction cells. In fact, high generation current densities along with high open circuit voltages have been reported for P-N junction solar cell structures fabricated incorporating violet-cell and textured surface techniques.

It is often stated (or implied) that Schottky cells are easily fabricated, giving an inherent processing simplicity (and cost) advantage over junction cells. This is a major misconception. Schottky cells require precise control of metal depositions in the thickness ranges of less than 100A in order to optimize trade-offs between conductivity and reflectance. Such control is difficult by evaporation, and more controllable sputtering techniques have resulted in lower open circuit voltages, presumably due to penetration of sputtered atoms through the interfacial layer into the silicon.[19] Yield, efficiency, and cost problems can be expected to continually plague this fabrication step. Schottky-type solar cells require the same highly conductive metal collection grid and anti-reflection coating deposition as do P-N junction cells. Rather than being simpler, the fabrication complexity for a good silicon Schottky solar cell would be about the same that of a good silicon P-N junction solar cell. It is Motorola's conclusion that the technological uncertainties that must be resolved in order to demonstrate the (slight) theoretical advantages of the silicon Schottky solar cell are much too great to permit considering it as a serious contender at this time.

6.1.7.1 SCHOTTKY BARRIER SOLAR CELL BIBLIOGRAPHY

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6.2 PROCESS ADAPTATION AND TECHNICAL ASSESSMENT

A major portion of the contractual effort involved a technical assessment of potential process steps for manufacturing silicon solar cells. First, a matrix of possible processing steps was assembled. Second, a group of evaluation criteria was defined to allow a technical evaluation of the usefulness of each individual process step when examined as an isolated step for manufacturing solar cells. Most of the individual process steps were then evaluated, either directly in the laboratory or through indirect methods such as literature

surveys, vendor contacts, and detailed discussions with process engineers in the Motorola manufacturing and research areas (for both discrete and integrated circuit products). This technical evaluation process resulted in the categorization of these individual process steps to reflect both technical readiness and an estimation of future technical utility. This section identifies the various process steps, their evaluation, and their technical categorization.

6.2.1 EVALUATION CRITERIA

Evaluation criteria were established to consider both the individual process step itself and also effects on properties of a solar cell resulting from its incorporation in the cell manufacturing sequence. Among the evaluation criteria were:

- Cost
    - Labor
    - Material
    - Capital
    - Expense Items
- Performance
- Controllability
- Amenability to automation
- State of readiness
- Reliability considerations
- Amenability to future sheet (ribbon) geometries.

Whenever applicable, each of these criteria was applied to both the process itself and to properties of the resulting solar cell. A poor rating in either case would result in an overall unsatisfactory rating. Performance of surface lapping silicon, for example, is judged favorably as an isolated process step,

but lapped silicon is rated poorly as a starting surface when considering its effects on solar cell performance. It must be understood that process steps do not stand on their merits as individuals, but on their ability to contribute synergistically to a process sequence. Each step must, then, be evaluated first, by itself, and second, as a member of a process sequence.

In this technical evaluation phase, cost criteria were applied in only a qualitative manner, reflecting only estimated and relative costs of competing processes. A detailed process step cost study was subsequently performed, and is reported in a later section.

The only other criterion which may not be self-explanatory is that involving sheet geometries. This requires an evaluation of a process step's suitability for application to a sheet which may have an irregular shape and also may be non-planar in nature. The sheet may, for example, be a ribbon which varies in edge shape, has surface ripples, and is warped. Some processes are relatively insensitive to these factors, while others become virtually useless. As-grown sheet is considered as having more severe geometrical problems than large area sliced sheets, which may also be utilized and must be considered as potential long-range substrates.

6.2.2 TECHNOLOGY ASSESSMENT CATEGORIES

A set of initial technology assessment categories was established at the beginning of the program. During the course of detailed process step evaluation, the set of categories was modified to reflect more accurately the requirements for evaluation of projected usefulness. The updated categories were as follows:

Category 1: Processes which are judged unlikely to be utilized in any recommended process sequence.

Cateogry 2: Processes which appear to require a major technological advancement to ensure usefulness. Technology in these areas

must be continually monitored to assess future applicability.

Cateogry 3: Processes which appear potentially promising, but which have required evaluations or equipment not available during the time-frame of this contract. Additional efforts should be expended on these processes.

Category 4: Proven processes which have a high chance of successful incorporation into future process sequences.

6.2.3 STARTING CONDITION OF SILICON SURFACE

The starting condition of the silicon surface plays a critical role in subsequent processing steps and in cell efficiency.

6.2.3.1 SAWED SURFACE (CATEGORY 1)

It is unlikely that silicon will be utilized in the as-cut condition. Although this form of silicon is the cheapest available today, near-surface damage (and possible contamination from the saw blade and coolant) can badly degrade the crystal properties upon subsequent processing. Heating of the sawed surface can result in polyganization or recrystallization, converting the area in which the p-n junction is to be formed into a polycrystalline region. Heating may also propagate surface damage far into the bulk, resulting in a heavily dislocated, low lifetime material. All of these factors can degrade efficiency in a severe, uncontrolled manner.

One possible exception to this conclusion exists, however. Severe surface damage may be utilized to getter undesirable impurities from the bulk silicon below. High temperature annealing of a sawed surface may produce this desirable result. Subsequent to annealing, an undamaged silicon surface could be revealed by etching the sawed surface, hopefully removing both the

damage and the impurities. There is at this time insufficient information available to draw conclusions; additional studies should be undertaken.

6.2.3.2 SAWED AND ETCHED SURFACE (CATEGORY 4)

This is the best candidate broadly available today. Etching is utilized to remove the sawing damage and contamination. Etching wafers can leave surfaces that contain only gradual undulations of a magnitude so small that no pattern having linewidths of interest to solar cell production should experience any masking difficulties because of surface non-planarity. Thus, apart from the future realization of direct sheet growth, this combination produces the cheapest material suitable for solar cells and has indeed been used to manufacture solar cells. Sawing kerf loss, and material removed by etching, are major drawbacks, however, to this being the most economical approach for long range utilizaton.

6.2.3.3 LAPPED AND/OR POLISHED SURFACE (CATEGORY 1)

Lapping produces a matte appearing surface on a silicon wafer. It will be a flat surface, and, if done carefully, both sides of a wafer can be made plane and parallel by lapping them both. Lapping doesn't necessarily produce a surface having less damage than careful sawing, but a sawed surface will not be as flat as a lapped surface. This process is slow, batch orientated, and labor intensive, and hence is too expensive for ultimate solar cell use.

Polishing is a process like lapping, in which successively finer grit media are used to end up with a mirror-flat scratch-free surface. This degree of smoothness is necessary in order to obtain, by photographic means, the very fine line geometries utilized on many semiconductor devices and integrated circuits. However, solar cell geometries are about an order of magnitude coarser, so polished surfaces are not required for solar cell processing even

where patterning is done photographically. Furthermore, polished surfaces typically contain more mechanical crystal damage than etched surfaces, making them potentially less satisfactory for solar cell use.

Both lapping and polishing are too costly for incorporation into a process sequence to make inexpensive solar cells.

6.2.3.4 CLEAVED SURFACE (CATEGORY 2)

Direct cleaving of silicon wafers or sheets from crystals would eliminate kerf losses, and could possibly produce smooth surfaces directly. To date, however, no process has been developed for cleaving wafers from a boule with anything approaching a satisfactory yield. If a major breakthrough in this area could be realized, it would be very cost competitive. No work appears to be currently underway in this area, however.

6.2.3.5 AS-GROWN SHEET SURFACE (CATEGORY 2)

This is the responsibility of several contractors in the LSSA Program Task II. Breakthroughs in technology are still required to make as-grown sheet practical in the large scale necessary. However, judging by the progress made to date, and the potentialities of the process, it must be assumed that the probability of success is high. The various processes being studied all have the possibility of providing as-grown surfaces suitable for efficient solar cell processing.

The geometrical variations in silicon sheet, however, can greatly influence the usefulness of some solar cell processing, fabrication, and encapsulation choices. It must be made clear that two separate philosophies may be pursued. The first simply states that the large area sheet must conform to certain geometrical limits in order to allow solar cell processing and encapsulation to be performed by essentially conventional silicon wafer processing methods.

The second, the converse of the first, states that whatever the shape that results from the sheet growth method, it will be used, forcing solar cell processing and encapsulation to conform to the delivered geometry.

The most likely ultimate choice, of course, will be a compromise between the two extreme philosophies in order to achieve cost effectiveness. The compromise may, however, provide non-planar, rough surfaced sheets as compared to today's surface texture and flatness standards for wafers. Accordingly, later processes which are recommended under this Task IV study must have the flexibility of handling such future material, or must be clearly labeled as applicable only to optimum surfaces.

6.2.3.6 TEXTURE-ETCHED SURFACE (CATEGORY 4)

Texture-etching has been shown to be a repeatable and uniform process on (100) oriented silicon surfaces. Texture-etching can be performed on any of the previously discussed silicon surface conditions. Costs of texture-etching are equal to, or less than, those for other techniques for silicon etching, producing silicon costs only marginally above those of present sawed and etched wafers. For this additional cost, a surface with distinct optical advantages (and attendant efficiency increases) is produced. The textured surface is dramatically different in nature from polished or etched surfaces now used widely in the semiconductor industry. This requires certain modifications of other steps in a process sequence utilizing textured surfaces. These modifications are easily achieved.

The main caveat which must be kept in mind is that texture-etched surfaces currently require (100) oriented surfaces. If future sheet processes cannot produce (100) surfaces, texture-etching development must be attempted for other silicon orientations. If, in the future, a choice must be made between two

sheet growth processes of otherwise similar properties, the advantage will lie with the sheet process which can be texture-etched.

6.2.4 IN-PROCESS SURFACE CLEANING OR ETCHING

Any solar cell manufacturing process will require cleaning steps at some stages. Further, most manufacturing sequences will require etching steps.

6.2.4.1 WET CHEMICAL CLEANING OR ETCHING (CATEGORY 4)

Processes in this category are widely utilized in the semiconductor industry with a high degree of success. Several major concerns exist at this time, however. First, it is possible to have unwanted contamination from wet chemicals. For any given process sequence and for each different manufacturing area, control limits will have to be defined for possible contaminants. At this time, no difficulties are seen in this area. Second, the use of wet chemicals limits the level of future cost reductions to the cost of those chemicals consumed, a serious limit if large quantities of chemicals are required. (This must include D.I. water which is consumed in rinsing after wet chemistry steps.) A third consideration is the disposal of waste chemicals. This can contribute additional materials and facilities costs to the utilization of wet chemistry. Nevertheless, because of its current strong position in the semiconductor industry, wet chemistry must still be considered a major possiblity for future use.

6.2.4.2 PLASMA CLEANING OR ETCHING (CATEGORY 4)

This is a dry process incorporating an RF field to excite a plasma. The energetic plasma is then used to remove material from the surface, either

through bombardment by inert energetic plasma ions, or by reactive ions liberated from molecules injected into the plasma. Based on their increasing acceptance by the semiconductor industry, plasma etching and cleaning steps have a high likelihood of supplanting at least some of the more traditional wet chemistry process steps.

A silicon nitride film for example, may be patterned utilizing a plasma etching process with excellent results. The plasma etching process, when compared to the wet chemistry process for etching, is less complicated and less time consuming. After application, alignment, and development of a photoresist film, etching of the exposed dielectric requires the following steps for the plasma and wet chemistry processes:

PLASMA	WET CHEMISTRY
Load in etch carrier	Load in etch carrier
Etch in plasma	Etch in solution
Remove photoresist	Rinse in D.I. H_2O
	Dry
	Remove photoresist

Not only is the plasma step simpler, it consumes only a small amount of material (etching gas) as compared to consumed acid and D.I. water for wet chemistry etching.

Plasma removal of photoresist ("ashing") has a similar appeal for process simplicity and consumed materials. Photoresist materials have notoriously contained metallic contaminants which, if left on the wafer surface and heated in subsequent process steps, could migrate into the silicon and degrade minority carrier lifetime. It is possible that photoresist removal by plasma techniques alone could leave such metallic impurities on the wafer surface. Evaluation of this aspect of plasma processing for solar cell fabrication, where high lifetime must be maintained, must be performed at a future date.

6.2.4.3 VACUUM BAKING AND REVERSE SPUTTERING (CATEGORY1)

While results are reportedly adequate, the comparative capital costs are prohibitive for further consideration.

6.2.4.4 TEXTURE-ETCHING (CATEGORY 4)

Rather than texture-etching as a pre-processing step, it can be incorporated within a process sequence. The previous discussion is applicable here.

6.2.4.5 CLEANING BY SCRUBBING (CATEGORY 4)

A technique relatively new to the semiconductor industry is cleaning of silicon wafers by the mechanical scrubbing of their surfaces with brushes. Until recently, such scrubbing was avoided to eliminate possible mechanical damage to the silicon surface. Studies have shown, however, that removal of tightly adhering (and otherwise difficult to remove) dirt particles can be achieved through scrubbing without silicon damage. The removal of these particulates is seen to improve process control, device quality and performance, and overall process yield.

Mechanical scrubbing, however, may not be possible on warped or rippled surfaces such as may be forthcoming from future large area sheet production, or on textured surfaces which may house impurities in valleys too tiny to be effectively reached by brush bristles. Manufacturers have recently indicated, however, that cleaning equivalent to mechanical scrubbing may be accomplished hydraulically with a pressurized spray of water.

Numerous vendors now have automatic and semi-automatic scrubbing equipment of both types available. Yield increases of several semiconductor lines within Motorola (precise data is considered proprietary) indicate that scrubbing is technically advantageous.

6.2.4.6 GAS STREAM DRYING (CATEGORY 4)

Wet chemistry steps reqire a subsequent drying operation. Drying by exposure to a (hot) gas flow has been one of the standards in the industry. It is forgiving of shape and is the prime contender for sheet geometries.

6.2.4.7 GRAVITY (CENTRIFUGE) DRYING (CATEGORY 4)

For round wafers, centrifuge or "spin" drying has become another of the semiconductor industry standards. In that industry, wafers are thicker and smaller than those likely to be utilized for future solar cells. This technique may require special adaptation for very large area, thin solar cell substrates such as long ribbons.

6.2.5 LIFETIME ENHANCEMENT AND PRESERVATION (CATEGORY 3)

Solar cell processing may require minority carrier lifetime improvement of the starting material, and must incorporate special precautions (and possibly specific techniques) to preserve lifetime during processing. Such processes fall into four general categories of lifetime enhancement: Complexing and removal of impurities, temperature-time profiling, leaching, and precipitation of impurities on damage sites or defects.

A literature survey on gettering of impurities in silicon has been performed; initial observations are that a variety of gettering processes has been investigated, and that the technology of impurity gettering is complex and far from developed to its full potential. In short, these processes all fall precisely within the definition of Category 3. Future efforts must be directed toward this area. A brief review of gettering is given here, followed by a bibliography of gettering references.

6.2.5.1 LITERATURE SURVEY OF GETTERING

In original investigations[1] into the removal of metallic impurities from silicon, the basic approach was to grow (or deposit) some type of oxide layer onto the surface of the silicon. The basic idea was that at high temperatures, the metallic impurities would diffuse to the surface and become trapped in the oxide layer. Various oxides, including phosphorus -, boron -, vanadium -, and lead - silicon oxides, were used. It was found that phosphorus glass did the best job.

Since then, studies[3,10,13] have shown that the metallic impurities are not gettered into the phosphorus glass, but instead are gettered to the heavily doped silicon under the glass. Apparently, the mechanism is one of increased solubility of metallic impurities in the phosphorus-doped silicon. Removal of impurities from the silicon, thus, requires removal of not only the oxide layer, but also the surface layer of silicon itself.

Normally, in bipolar processing, phosphorus gettering is used to transport metallic impurities away from active device areas to an unused portion of the wafer (i.e., the isolation diffusion or the back of the wafer). In MOS processing, a phosphorus glass is deposited on top of the passivation oxide to getter sodium impurities from the gate oxide[11]; this glass, however, appears to do little gettering of metallic impurities from the bulk of the silicon.

It has also been shown that a preoxidation gettering of the backside of the wafer will reduce the generation of oxide-induced stacking faults[14] (OISF). It is believed that OISF act to precipitate metallic impurities and thus degrade device characteristics. It is also believed that OISF are sites of enhanced phosphorus diffusion, and thus cause emitter-collector piping defects in bipolar devices.

It has been found that the use of various chlorine compounds during oxidation will getter both metallic impurities from the bulk silicon [4,7,8] and sodium impurities from the oxides that are grown[5,6,9,12]. Chlorine gettering can be used only during oxidation because it could otherwise cause extreme etching and pitting of the silicon[4]. Chlorine gas has been used with some success, but it may cause etching of the silicon. Hydrogen chloride has been the most successful gettering compound.

The chlorine gettering mechanism is believed to be diffusion of metallic impurities to the surface, followed by formation at the surface of volatile metallic chlorides which are then carried away by the gas flow. The gettering effect improves with increasing temperature (especially above $1000^{\circ}C$) and increasing amounts of HCl. The limit to the amount of HCl used occurs when significant etching of the silicon begins, or condensation of hydrochloric acid droplets takes place in the cooler portions of the furnace tube. The optimum mixture of HCl is about 5 - 10% HCl by volume in dry O_2.

It has also been discovered that the use of HCl will clean the furance tube of metallic impurities, and thus reduce contamination from that source to virtually nil[6]. The process used is 10% HCl in dry oxygen at $1150^{\circ}C$ for 6 hours.

It should be noted that the use of HCl with steam instead of dry O_2 will still getter Na and the oxides thus grown, but will not as effectively getter the metallic impurities from the bulk. It is believed that the accelerated oxidation of metallic impurities in steam inhibits the formation of volatile metal chlorides.

It is well known that various types of crystallographic defects in silicon will tend to precipitate metallic impurities. This principle has been used to getter impurities by deliberately introducing defects in the back of the wafer, using them to trap metallic impurities migrating from the active device

regions. It should be emphasized that this method does not remove metallic impurities from the wafer, but merely moves them around. Methods of introducing defects include mechanical abrasion and ion implantation of Ar, O, P, Si, As, or B. As was suggested earlier, sawing damage may also be an appropriate starting point.

Boron diffusions have been used to getter metallic impurities from silicon, but are not as effective as phosphorus[3]. The mechanism is apparently the formation of metal precipitates, rather than any increased solubility of pairing.

Some gettering action has also been observed with the use of Si_3N_4 layer[18]. Gettering can also be achieved through the appropriate use of controlled heating and cooling rates, and the temperature range of controlled heating and cooling. These cycles apparently function through a precipitation process, removing impurities from electrically active sites.

Since solar cell efficiency is extremely dependent upon lifetime, gettering cycles to improve or preserve lifetime seem appropriate for future incorporation into solar cell process sequences. The exact choice (or choices) will require further experimental work, however.

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6.2.6 JUNCTION FORMATION

The most complex and critical steps in solar cell processing involve junction formation. In order to stay within the design requirements of an efficient solar cell, the junction depth must be controlled to be consistently less than 0.5 micrometers, and preferably less than 0.2 micrometers. This places stringent control problems on the techniques utilized for junction formation.

6.2.6.1 EPITAXY (CATEGORY 1)

Motorola has obtained long and continued experience in automated silicon epitaxial growth. Silicon deposition is accomplished in RF-heated, cold-walled chambers by chemical vapor deposition at temperatures near 1100°C. Present and projected state-of-the-art have shown that accurately controlled deposition of silicon at thicknesses of (or below) 0.25 micrometers will be impractical. In this range, thickness is difficult to control. Interdiffusion of impurities is appreciable at these high deposition temperatures, resulting in further control difficulties, and degrading performance. Projected yields and resulting costs make this method unlikely.

The only foreseen possibility is a low temperature plasma-aided or vacuum-aided deposition. At this time, these processes are considered speculative.

6.2.6.2 DIFFUSION (CATEGORY 4)

Diffusion is a generic term utilized to describe thermal motion of impurities employing a broad variety of doping techniques. Diffusion is normally accomplished by deposition of a shallow (source) region of impurity in the silicon, followed by a high temperature redistribution; these items take place either sequentially or simultaneously. All diffusion processes

have the common feature of rather isotropic introduction of a dopant into exposed surfaces, with first order junction depth control being accomplished by time and temperature. Control of surface concentration is commonly obtained by utilizing solid solubility of an impurity in silicon to establish an easily controlled impurity source. Temperature is frequently utilized as the controlling parameter for the level of solid solubility, lower doping levels occurring at lower temperatures. Since diffusion is a high temperature process, unwanted effects contributing to reduced lifetime can occur during the high temperature exposure. For example, fast-diffusing impurities serving as efficient recombination centers in the silicon lattice can be accidentally added; crystal structure deterioration, particularly at near-surface regions (e.g., oxidation-induced stacking faults and their subsequent evolution into more complex defects) can be introduced; and oxygen precipitates of various types can be formed. Hence, choice of a diffusion process sequence must consider the resultant lifetime that can be reproducibly obtained, as well as the formation of the P-N junction itself.

Deposition of diffusion sources by chemical vapor deposition (CVD) or by vapor transport are the most widely utilized techniques in the semiconductor industry. These technologies are fairly mature and have been successfully applied to the fabrication of high efficiency solar cells.

Spin-on application of diffusion sources is also commonly used in areas of the semiconductor industry today as an alternative to the more conventional gaseous carrier methods. Further, spin-on diffusion sources can be utilized as antireflection coatings on solar cells.

Most present uses of spin-on diffusion sources are on round wafers which can be readily spun at high speeds during application. Such spinning processes may not be transferrable to rectangular ribbon or very large sheet geometries, but may require spray-on or roll-on technology to be developed. Other than the

exact application method, however, the remainder of the technology should be directly applicable to future geometries.

Typical spin-on sources consist of a solution of an organic silicate, an alcohol, and a small proportion of an organic compound of the desired dopant element. The liquid is usually filtered, and is in the form of a solution rather than a suspension. It is applied to the wafers using standard photo-resist spinners. Subsequent heat treatment forms a doped silicon oxide layer on the surface of the wafers, the organic components of being driven off. [1] This densified layer acts as the dopant source during diffusion.

Spin-on diffusion sources can be formulated for specific dopants and dopant concentrations. [2, 3, 4] In addition, as is the case for gaseous diffusion sources, sheet resistivity and junction depth can be controllably varied by changing the diffusion temperature and time. Dopant surface concentrations have been varied up to solid solubility and have been controlled experimentally by the dopant concentration of the spin-on film. [4]

Wafer-to-wafer dopant uniformity has been shown to be excellent. A lot of 52 wafers, for example, boron diffused from a spin-on source showed a mean standard doping deviation of 3%. [5] Production performance has also been tested on small signal PNP transistors manufactured solely from spin-on sources. Such transistors met all the DC electrical specifications for devices manufactured from conventional gaseous diffusion sources. [6]

Since diffusion occurs from a doped oxide film, diffusion of different dopants and/or concentrations can be performed simultaneously on opposite sides of the wafer without concern for cross-contamination. This feature could allow, for example, P-N junction formation simultaneous with back surface field diffusion.

Textured silicon surfaces, as well as ribbon or other surfaces with irregularities in the macroscopic range, may cause some problems with spin-on diffusion sources. It is possible, for example, that the pyramids of a textured surface

might cause uneven film thickness, being thicker than average in the valleys between pyramids and being correspondingly thinner at the tips of the pyramids.

All of these considerations indicate the need for studies of alternate spin-on diffusion source application methods.

SPIN-ON BIBLIOGRAPHY

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6.2.6.3 ION IMPLANTATION (CATEGORY 4)

Ion implantation of the dopant, unlike diffusion, is not isotropic, but is unidirectional, with depth dependent upon implantation energy. Ion

implantation can be performed with extremely pure, mass analyzed dopants, avoiding any undesired contamination. Surface concentration can be controlled by ion dose. The main drawback to ion implantation is the high capital cost. Ion implantation may be utilized to form the P-N junction directly, or the implanted layer may serve as a well-controlled source of impurity for a subsequent diffusion step. If a subsequent diffusion is not performed, the implanted dopant must at least be activated by a high temperature anneal. This temperature may be as great as 900°C if resistance furnace heating is used and high doping efficiency is to be maintained.

For solar cell applications, throughput is dependent on ion beam current. Machine technology has progressed to the point of producing sufficiently high dopant ion beam currents to be a serious contender for solar cell processing. Still greater beam currents appear feasible, making ion implantation compatible with the longer range LSSA Project cost goals.

As will be discussed in a later section, efficient solar cells have been fabricated at Motorola utilizing an ion implanted junction, establisning ion implantation as a viable process technique for P-N junction formation.

6.2.6.4 ALLOY (CATEGORY 1)

This original technique for P-N junction formation was largely bypassed by other processes due to its lack of control and its intractability for anything but simple patterning. For solar cell use, the alloying material would have to be removed, exposing the (liquid phase epitaxy) regrown region below. Since the surface region is grown from solution, its impurity profile may not be controlled as desired to produce a drift aiding field. There appears to be no new development on the horizon to create renewed interest in alloying for solar cell P-N junction formation.

6.2.7 CONTACT METALLIZATION

Metallization constitutes the interface between the silicon and the module and because it is a critical interface, often determines both module performance

and module reliability. On one hand, solar cell contact metallization must cover the minimum possible area while achieving minimum resistance. On the other hand, the metallization must provide excellent mechanical adherence to the cell in environments which contain moisture, apply mechanical stress and in some applications, experience high voltage between solar cells and the package. The metallization system is almost always involved in the failure of semiconductor components, and it is expected to be a critical component of solar module reliability.

6.2.7.1 VACUUM DEPOSITION (CATEGORY 1)

Vacuum deposition is the predominent metallization method utilized in the semiconductor industry. For most semiconductor devices and integrated circuits, a metal (or layers of metals) is deposited by evaporation or sputtering onto the entire wafer surface and subsequently patterned into small geometries in a photolithography (photoresist) step. Solar cell metallization, on the other hand, employs a large geometry pattern with (by comparison) coarse lines. Some patterns can be made amenable to evaporation through a mask, thus eliminating the photoresist step. Totally redundant multiple contacts cannot however, be patterned through a metal mask if all metallization lines are to be directly interconnected on the cell surface. (Portions of the masking pattern would be unsupported and would fall out.) Evaporation through a mask and photolithographic removal are both very wasteful of material, typically utilizing no more than 5% of the metal consumed. Further, both processes require further chemical consumption for etching the excess metal, either from the wafer or the evaporation mask. Capital cost of vacuum equipment is higher than that for any other metal deposition technique. Vacuum deposition is not expected to be a viable contender for future solar cell application. (A more detailed discussion of cost information is presented in Section 3.6.)

6.2.7.2 PLATING (CATEGORY 4)

Plated contacts which satisfy all contact metallization criteria have been produced in the Motorola Solar Energy R&D Laboratory. Accordingly, plating is considered to have a high probability for future usage in solar cell contact metallization. Plated contacts are amenable to automation. Costs for materials are moderate, but labor and capital costs are low. Most important, plating is the most forgiving of all metal processes to surface and geometrical irregularities.

6.2.7.3 CHEMICAL VAPOR DEPOSITION (CATEGORY 1)

Chemical vapor deposition of metal contacts employs the decomposition of a metal-bearing gaseous compound, often in the presence of a second gas. Primary candidates are metal-organic compounds (which are generally very expensive) and material waste is appreciable. It is doubtful that cost savings over established vacuum technology can be realized. Metallization by means of chemical vapor deposition should be considered only via an evolution of potentially useful new systems, decreased raw materials costs, and improved material utilization.

6.2.7.4 PRINTING (SILK SCREENING) (CATEGORY 4)

Printed contacts are painted (and simultaneously patterned) directly onto the silicon solar cell surface. Printed contacts for solar cells have considerable appeal due to the possible lower cost of this approach when compared to more conventional methods of contacting silicon, such as metal evaporation or sputtering. The printing process itself is not only fast, but the capital cost of equipment is low. The line widths required for solar cells are close to the limits of resolution for printing, however, and may limit its use to plane surfaces.

Printed contact materials utilize a carrier or binder. Following application, printed contacts must be heat treated ("fired") to promote electrical contact and physical adhesion to the silicon, and to enhance conductivity of the film. The carrier is removed during firing, but it still must be inert with respect to the silicon so that junction quality is preserved.

Adhesion and contact resistance of printed contacts require special attention. Typically, present printed metal systems are either copper or silver based, and have been designed for adherence to ceramic parts rather than silicon surfaces. Since neither copper nor silver forms inherently strong mechanical bonds with silicon, adhesion may be promoted through the incorporation of glass frits into the printing material; these frits sinter to an oxide film on the silicon surface. Incorporation into the printing material of other metals, in addition to frits, is also utilized in an effort to enhance adhesion. The dependence of glasses for adhesion of printed contacts can produce unsatisfactorily high electrical contact resistance due to reduced metal-silicon contact area. Trade-offs occur, thus, between frit quantities, silicon surface preparation, metal combinations, metallization patterns, and contact firing temperatures. It has been observed that low temperature firing of contacts will result in poor contact adherence and poor interconnection reliability, while high temperature firing can generate yield and efficiency losses due to alloying, shorting, or lifetime degradation when applied over very shallow p-n junctions.

Six conductive ink samples were given a preliminary evaluation during this program period. They are formulated and classified as:

1. Silver with frit
2. Silver without frit
3. Silver with 2% palladium with frit

4. Silver with 2% palladium without frit

5. Silver with 2% platinum without frit

6. Copper with frit

In order to evaluate contact resistance and adhesion, these samples were applied to silicon surfaces with both an intentional oxide thickness and a minimum oxide thickness. In the first case, a layer of silicon dioxide was formed in the contact areas to a thickness of approximately 100A. This thickness of SiO_2 is slightly greater than that which would normally form on a silicon wafer which has been stripped and exposed to the ambient for a period of several days. The metal inks were then applied and processed according to the manufacturers' suggested temperature cycles to test their ability to penetrate a native layer of SiO_2. The second case, contact areas were cleared with hydrofluoric acid, rinsed, and dryed immediately prior to conductive ink application. This technique produces the minimum possible oxide thickness under the metal without the use of vacuum techniques; it provides that thickness of SiO_2 seen in most semiconductor industry metallization processes.

In order to reduce the influence of other unwanted variables, all six formulations were applied to individual large area planar diodes on a single silicon wafer. The diodes were approximatley $2.5cm^2$ in area with a contact area approximately $0.2cm^2$. All diodes were N on P, with the P-type substrate common to all diodes. The diodes were fabricated by ion implantation and had textured surfaces. The junction depth under each contact area was greater than that of the surrounding areas, being near 1.2 micrometers. As N-type regions of the diodes were electrically isolated from each other, it was possible to process the wafer as a unit and perform testing on the individual segments without scribing or otherwise interfering with the integrity of the wafer.

Firing temperature cycles utilized were those suggested by the manu-

facture of the silver containing formulations, and below the recommended 600°C to 1000°C firing temperature for the copper formulation. The temperature rise and fall rate was approximately 50 degrees per minute, and the peak temperature was 550 degrees C. The atmosphere was air, and the wafers were allowed to stay at the final temperature for three to five minutes. After firing, the wafer segments were tested for adherence, and electrical parameters were measured to evaluate series and shunt resistances resulting from poor ohmic contact or diode degradation respectively.

Adherence of the inks to the diodes was first observed. As anticipated, the copper formulation showed extremely poor adherence and will have to be treated separately. All five of the silver formulations, however, showed reasonable physical adherence in a "Scotch tape test".

The electrical performance of each ink was then evaluated. None of the inks showed significant penetration through the intentionally formed SiO_2 layer, while all exhibited electrical contact to the HF etched surface. This indicates that storage without an etching step immediately prior to ink application is inadvisable.

With freshly-etched surfaces, the series resistance was frequently high, indicating that either a high contact resistance was present or that the applied layers were too thin to adequately carry the desired current. The former possiblity implies the desirability of a more controllable formation and/or a more severe heat treatment. The latter suggests either a thicker layer or a subsequent solder coating. In none of the above experiments was any significant degradation of the diode characteristics due to shorting or lifetime killing observed.

Among the unknowns of printed metallization is the long term reliability of modules operating in the terrestiral environment, and how this depends on processing and formulation variables.

It is a current conclusion that extensive developmental work on printable contact metallization formulations for silicon solar cells is needed. Attendant to this formulation development is the necessity for further process definition and development for solar cell application. A basic understanding of printed contact-silicon interfacial physics should be obtained. Sufficient promise exists for such commitment.

6.2.7.5 LAMINATION (CATEGORY 2)

The attachment of pre-shaped metallization patterns by lamination, such as a tape transfer technique, is also potentially attractive. Further development is necessary before it can be considered viable. Potential problems are similar to those facing printed metallization. No lamination research is being reported at this time.

6.2.7.6 SOLDER COATING (CATEGORY 4)

In many cases, solar cell metallization systems will be composed of a base metal system for electrical and mechanical contact to the silicon surface, and a solder coating which will be thick enough to act as the primary current-carrying metal. Sophistication of processing already exists in the solder coating areas, and little development work is required. However, it is necessary that the surface of the underlying metallization be amenable to controllable solder coating, implying that the soldering cycle may have to be tailored to the metallurgical properties of the contact metallization.

6.2.8 ANTIREFLECTION (AR) COATING

A necessity for achieving maximum efficiency from the solar cell is a high quality antireflection coating system. In some cases, this antireflection coating may be used for P-N junction passivation.

6.2.8.1 VACUUM DEPOSITION (CATEGORY 4)

The same basic comments made for metal vacuum deposition apply here, except that it is seldom required to pattern the AR film since it is generally

applied after metallization (a mechanical mask may be used to prevent AR film deposition on the bonding pad areas). Film thickness control is critical. While suitable technology is now available, other methods appear to be cost preferable. On the other hand, vacuum deposition is the best current method for applying some materials as AR films.

6.2.8.2 CHEMICAL VAPOR DEPOSITION (CATEGORY 4)

Silicon nitride could constitute an excellent choice for the anti-reflection coating on silicon solar cells. In addition to its useful refractive index ($n \cong 2.0$), it is the best silicon P-N junction passivant known to the semiconductor industry. It is extremely stable and inert. Silicon nitride can be deposited by low temperature CVD processes in a "soft" state which permits easy patterning using standard SiO_2 etching processes, and then can be transformed by a modest thermal cycle into its high density state. The CVD process could be much cheaper than a vacuum deposition process, and comparable to (or cheapter than) a spinning process if the deposition reactor capacity can be made large.

Silicon nitride has been deposited at $600^{\circ}C$ in a hot wall, quartz lined furnace. The nitride is deposited from the reaction of silane (SiH_4) and ammonia (NH_3) in a nitrogen carrier gas. Deposition cycles of approximately 50 minutes have resulted in silicon nitride layers of $1050A^{\circ} \pm 100A^{\circ}$, this excellent uniformity applying to both variations within a run and variation from run-to-run. As established, the process deposits the nitride on wafers placed horizontally in the furnace; as a result this deposition system is capable of processing only five 3" wafers per run. This low throughput would be unacceptable for long range LSSA Project goals.

As an alternative deposition approach, greatly increased area throughput has been reported by silicon nitride deposition at a reduced (less than 1 atmosphere) pressure. Such a system has been utilized to simultaneously coat

seventy-five 3 inch diameter wafers with silicon nitride films having a thickness uniformity of ±5%.

6.2.8.3 DIRECT GROWTH (SiO_2)(CATEGORY 1)

The index of refraction of SiO_2 is essentially equal to those of all of the proposed encapsulant materials, making purposeful growth of SiO_2 as an AR coating unnecessary. If bare cells are considered, the SiO_2 would be a reasonable AR material. If it forms a better surface material for encapsulant bonding in a package, SiO_2 may be reconsidered; this event is considered unlikely.

6.2.8.4 PLASMA DEPOSITION (CATEGORY 2)

Deposition of antireflection dielectric coatings can be performed by plasma-aided CVD reactions at much lower temperatures than are possible by thermally activated CVD. This area is receiving considerable attention by the semiconductor industry, but it still needs technological advancment prior to extensive consideration for the LSSA Project.

6.2.8.5 SPIN-ON OR SPRAY-ON DEPOSITION (CAGEGORY 3)

Antireflection coating compounds can be applied in the same manner as photoresist, followed by a bake cycle to complete chemical reactions and/or to drive off solvents. Further heat treatment is frequently necessary to densify the film in order to realize optimum optical properties of the material.

Spin-on sources to deposit antireflection coatings of tantalum oxide or titanium oxide have been commercially formulated. As an example, a single application of spin-on can give a TiO_2 film which can be patterned in the as-

deposited condition. Following a 925°C densification, it has a thickness ranging from 800 to 1100A, is resistant to HF etching, and has an index of refraction of approximately 2.0. Application following metallization requires much lower temperature annealing steps. 250°C for 30 minutes can be used to give an AR coating of usagle quality; reliability of such low temperature-fired films needs to be ascertained.

While spin-on antireflection coatings may be useful on round, polished wafers, they will most likely be unsatisfactory for solar cells of rectangular shape or with surface roughness (either ripple, an as-grown surface, or a texture-etched surface). As discussed in Section 6.1.6, photoresist application by spinning on textured surfaces results in non-uniform thicknesses of photoresist over the surface features. It is anticipated that future application of this type of antireflection coating must be by spray-on techniques. At this point in time, it appears that spray-on thickness control and uniformity are not suitable for quality antireflection coating.

6.2.9 ANNEALING

All solar cell manufacturing process sequences require some high temperature annealing.

6.2.9.1 RESISTANCE FURNACE HEATING (CATEGORY 4)

This is the almost universal semiconductor industry tool. As currently utilized, its energy consumption is high. However, in a continuous, automated environment, the energy dissipation per unit area of silicon is capable of appreciable reduction from today's practices. Uniformity and control exist now, even for large area sheets, and the technology is proven.

6.2.9.2 DIRECT RADIANT HEATING:

HIGH TEMPERATURES (CATEGORY 2)

LOW TEMPERATURES (CATEGORY 4)

This technique has had only limited application in semiconductor technology for high temperatures, and has several inherent problems. The life of high intensity radiant sources is short, and output is somewhat variable during that lifetime. Uniformity and efficiency of heating require reflective surfaces for radiant energy manipulation; these can also degrade with use. When employed for high temperature (where radiant energy absorption is good) heating of silicon, direct radiant heating of large areas to a specific temperature is hard to control. Major technological advances are required for high temperature applications.

Low temperature applications, such as for solder reflow or photoresist baking, are well developed and are considered viable at this time.

6.2.9.3 LASER AND ELECTRON-BEAM HEATING (CATEGORY 3)

These emerging technologies show promise of excellent control and good efficiency. Application to semiconductor technology has been, however, limited, and requires further study before conclusions can be drawn. E-beam heating is being explored on another program under LSSA Task IV. Laser heating can be accomplished in any atmosphere, but E-beam heating must be performed in a vacuum.

6.2.9.4 RF HEATING (CATEGORY 1)

RF heating is broadly used in silicon epitaxy to obtain high temperatures in a "cold-wall" (and thus noncontaminating) system. Heating of the silicon for epitaxy is indirect, however, in that a conducting susceptor is first heated by the RF field; this susceptor, in turn, conductively heats the silicon.

This process is energy inefficient. A cold-wall system is not considered necessary for solar cell processing. Silicon wafers could be directly heated by RF energy, but the temperature control has been shown to be poor.

6.2.10 PATTERNING

Metallization, antireflection coatings, and dielectric layers for diffusion masks may require patterning in any given solar cell fabrication process.

6.2.10.1 PHOTOLITHOGRAPHY (CATEGORY 4)

Photolithography can be accomplished by either contact printing (direct mask contact to the silicon) or by projection or proximity (out-of-contact) masking techniques. Both proximity and projection require sophisticated optics, but can give extremely long mask life and well defined patterns on irregular surfaces. Both are far preferable, thus, to contact printing. In any case, mask alignment to the silicon substrate should be primarily mechanical, as opposed to optical, and realignments should be avoided if possible because they tend to be expensive. Exposure will continue to be by ultraviolet or visible light unless some technological breakthrough occurs in either laser, E-beam, or X-ray exposure. Application is expected to be limited to dielectric patterning.

6.2.10.2 SHADOW MASKING:

VACUUM METALLIZATION (CATEGORY 1)

PRINTED METALLIZATION (CATEGORY 4)

ION IMPLANTATION (CATEGORY 4)

This technique is too wasteful of material to be utilized for vacuum metallization of solar cells. On the other hand, planar P-N junctions can be formed by

shadow masking during ion implantation with excellent results and low cost. If planar junctions are utilized with ion implantation, masking will definitely be done by this technique.

Printed contacts are generally applied through a screen which, in effect, is a shadow masking operation. Printing contacts (in a manner analogous to operation of a printing press) would yield direct application in the desired pattern; this technique, however, appears to be receiving no current development.

6.2.11 INTERCONNECTION

Interconnections of solar cells into modules pose some stringent requirements for performance and reliability. The interconnection scheme must not contribute a substantial series resistance, or performance of the module can be seriously degraded. Experience derived from the semiconductor industry would suggest that metallurgical interactions are the most likely failure mechanisms. These can lead to reduced output, for example, as a result of increased series resistance, or interference with the optical path, or, perhaps more commonly, opened connections.

6.2.11.1 SOLDER REFLOW (CATEGORY 4)

The most widely used, and probably the most cost effective, solar cell interconnection scheme utilizes solder reflow. The technology is ready and has proven reliability. Properly applied, it can be used for the simultaneous formation of all interconnects in a module.

6.2.11.2 THERMAL COMPRESSION AND ULTRASONIC LEAD BONDING (CATEGORY 1)

Though widely used in the semiconductor industry, thermal compression bonding is useful mainly on small diameter (less than about 100μm) wires where deformation is accomplished by pressures low compared to the fracture

strength of silicon. Where millimeter sized bonds are required, this process is expected to be too damaging to the substrate to warrant further consideration.

Ultrasonic bonding is a low pressure process which utilizes ultrasonic energy to smear metal surfaces together, thereby establshing intimate contact for a metallurgical bond. It is not area limited, as is thermal compression bonding, but can damage substrates. It is also an unlikely future choice.

6.2.11.3 WELDING (CATEGORY 3)

Welded contacts are potentially as viable as those made by solder reflow. Welding, however, requires higher temperatures than soldering and can result in damage to the solar cell. Welding is used on small space cells, but its application to high current terrestrial cells will require additional innovation. Further detailed study is required before recommendation for future use can be made.

6.2.11.4 FILLED ADHESIVES (CATEGORY 2)

Metallic filled adhesives have had little or no application for bonding wires to solar cell metallizations. Filled adhesives are used in the semiconductor industry for relatively large area bonding (e.g., die attach). These materials have poorer electrical conductivities than metals, and the better ones (e.g., gold filled) are expensive. In a solar panel, where thermally or mechanically induced tensile stresses on the interconnect wires may be expected, the reliability of filled adhesive bonds is questionable. However, this field is continually changing, and should be monitored.

6.2.11.5 CLAMPED CONNECTORS (CATEGORY 1)

A direct clamping to the cell metallization is possible, especially if metal smearing at the contacts can be achieved without damage to the cell

itself and pressure can be maintained in the package. Without such smearing, moisture ingression to the contacts would increase resistance and reduce module reliability. Tooling would be expected to be complex to provide smearing without fracturing cells, with little assurance of control or reliability. This process is deemed unlikely to succeed for solar cells.

6.2.12 CATEGORY 4 PROCESSES

The processes which at this time appear to have a very high probability of incorporation into a future production process are tabulated here as a separate group of category 4 items.

1. Starting Condition
    a. Sawed and Etched Surfaces
    b. Texture-Etched Surfaces
2. In-Process Surface Cleaning or Etching
    a. Wet Chemical
    b. Plasma
    c. Texture-Etching
    d. Scrubbing
    e. Gas Stream Drying
    f. Gravity (Centrifuge) Drying
3. Junction Formation
    a. Ion Implantation
    b. Diffusion
4. Metallization
    a. Plating
    b. Printing
    c. Solder Coating

the cells, are insufficient to protect cell structures for long term terrestrial service. Until the MTBF of unencapsulated cells can be projected to 20 years, Motorola feels both front and back covers should be incorporated into the encapsulation system to meet the reliability goals of the LSSA Project.

It is anticipated that the most common failure modes for solar cell modules will be one of two types:

1. Failure of a solar cell interconnect within the package, as a result of strains due to thermal stresses or mechanical motion, or as a result of chemical or electrochemical corrosion.

2. Localized interference of the optical path, by delamination or physical coverage, i.e., by a leaf, localized debris, or wildlife.

6.3.1 INTERCONNECTION

The above failure modes are most severe for single contact, series interconnected cells, suggesting future use of both redundant cell contacts and parallel-oriented cell interconnections. In aiming towards an MTBF of 20 years, it must be expected that some interconnect failures will occur in a large array. In a series-connected panel, failure of an interconnect internal to the package (open circuit to either side of a solar cell) will cause entire module failure (open circuit). The use of redundant contacts to each solar cell will greatly reduce the magnitude of the effect of a single contact failure on the module performance. Instead of an open circuit, the output current will be reduced by some nominal factor (e.g., 5%, but dependent upon detailed cell design) if a single front surface contact opens.

Shadowing by relatively small objects is perhaps the most objectionable failure mode of the series-connected solar cell panel. Although intermittent, shadowing by leaves, debris, or wildlife on the external surface of a module

5. Antireflection Coating

   a. Vacuum Deposition

   b. Chemical Vapor Deposition

6. Annealing

   a. Resistance Furnace Heating

   b. Low Temperature Radiant Heating

7. Patterning

   a. Proximity Photolithography

   b. Projection Photolithography

   c. Ion Implantation Shadow Masking

8. Interconnection

   a. Solder Reflow

6.3 INTERCONNECTION AND ENCAPSULATION

In order to establish working systems of useful size, individual solar cells must be interconnected in some manner, and then encapsulated. Interconnection and encapsulation both play a major role in establishing (and enhancing) module reliability.

There is a trade-off between solar cell durability in harsh environments, and encapsulation requirements to protect the cell from these environments. This trade-off must be considered in terms of a minimum twenty year service life for the encapsulated cell.

The cost effectiveness of any particular encapsulation structure is heavily dependent upon the expected life (MTBF, or mean time before failure) of a totally unprotected cell as compared to the expected life of that cell within the encapsulation structure. It is presently felt by Motorola that single sided encapsulation structures, such as mounting on a glass cover, or using an epoxy-fiberboard substrate plus a silicone adhesive and covering for

will cause failure; almost total open circuit if an entire cell is shadowed, and reduced current output if the cell is only partially shadowed.

These types of failures may be alleviated by incorporating redundancy within a module through the use of a parallel or series-parallel cell interconnection schemes. Some schemes increase module (and system) reliability while insuring at least equivalent total system performance.

Any interconnection (and encapsulation) design, thus, should permit incorporation of some degree of parallel interconnections.

6.3.2 MODULE MATERIALS AND ENCAPSULATION

Materials must be chosen for solar cell modules, both for interconnection and for encapsulation, on the basis of functional compatability, long term reliability, and cost. The emphasis, while shared between these criteria, cannot compromise long term reliability. Accordingly, a set of encapsulant and interconnect materials was chosen for study on this program, with emphasis on proven histories of stability in terrestrial environments. Interconnection of cells is accomplished by solder reflow. The encapsulant system consists of a front glass cover, a stainless steel back plate, silicone potting, and a stainless steel bezel to act both as a structural member and as a sealing surface for formed-in-place gasketing. This structure has been shown to resist moisture ingression during stress testing as discussed in Section 3.4.4. The structure has good thermal dissipation and should offer long service life. Solar cell encapsulation has been successfully performed utilizing this system.

6.3.3 PROTECTIVE COATINGS FOR METAL ENCAPSULANT PARTS

A metal back plate may be utilized in encapsulating solar cells. It must be corrosion-resistant to achieve the twenty year life expectancy of

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the module. Both aluminum and stainless steel are possible materials, with stainless steel having the more suitable thermal expansion properties. Aluminum is particularly susceptible to corrosion in environments containing certain pollutants (e.g., salt, some industrial waste gases).

In order to reduce the overall cost of encapsulating solar cells, it would be desirable to utilize a material cheaper than stainless steel. Use of cold rolled steel would result in a savings of 5X (i.e., stainless steel = 60¢/ft^2 -- cold rolled = 12¢/ft^2). These prices reflect the cost of sheets 15 - 18 mils thick. It appears that cold rolled can be used if properly protected from the environment. A material, Rilsan Nylon II, has been used for approximately 25 years to coat items such as gas cylinders, underground piping, ship parts and outdoor furniture. It apparently has excellent wear properties for these and other applications. Application of the material is achieved by electrostatic spraying or fluid bed dipping followed by a heat treatment to fuse the powder. Electrostatic spraying can provide layers of approximately 3 mils while fluid bed applications have a minimum thickness of 8 - 10 mils. Material cost of 2¼¢/mil/ft^2 results in 7¢/ft^2 for the electrostatic process and 18¢ - 25¢ for the fluid bed process. Application costs range from 2 to 5 times material cost. Hence, electrostatic spraying of nylon on cold rolled steel could reduce costs and give acceptable long term reliability. Furthermore, numerous colors can be applied, thereby improving reflecting and radiating qualities of the package.

6.3.4 MOISTURE INGRESSION

Semiconductor industry experience on reliability and failure modes indicates that the solar cell metallization and interconnect system can be expected to be perhaps the region most vulnerable to failure resulting from package moist-

ure ingression. Absolute exclusion of moisture from a solar cell module for a period of twenty years would require hermetic seals, and hence would place severe economic strains on the encapsulation system. A far preferable solution would be a moisture resistant cell metallization and interconnect system.

Some current solar cell metallization systems, such as titanium-silver, have already shown reliability problems in moist ambients and would require special protection techniques to achieve a twenty year minimum service life. This is not unexpected from the experience in the semiconductor industry. Design choices for future solar cells should be based on metallization system reliability in moist ambients, and the final choice may be dictated primarily by this criterion.

It is not just moisture, but the combination of moisture and contaminants in the environment surrounding the metallization and contacts, and the effects of applied or generated electric fields and contact potentials, that must be considered. Even gold, which is considered to be quite inert, has been shown to exhibit severe degradation via electrochemical attack in plastic-encapsulated silicon integrated circuits, and also in hermetic packages that were sealed with some moisture inside.

A stress testing method for measuring moisture ingression into potential encapsulation and materials configurations has been investigated. The technique involves impregnation of color-indicating-dessicant materials into mock-ups of module designs. In a preliminary test, a color indicating dessicant was impregnated into a silicone potting compound in dummy modules with a glass cover and a stainless steel backplate. The modules were then boiled in water for times up to two weeks, periodically inspecting the dessicant. An approximate value for both interfacial and bulk moisture ingression can be obtained merely by visual inspection. This technique is one of those being utilized to evaluate encapsulation designs and materials.

6.4 COST ANALYSIS

Analysis of the costs of performing both individual process steps and process sequences was performed. This analysis was based upon today's technology projected to large volume production, and has been performed in a format conforming to the information chart utilized by JPL for summary of Task IV data. This format identifies the following items:

Material

Expense

Labor

Overhead

Interest

Depreciation

Capital Equipment

Facilities

The three primary assumptions made in this cost analysis are:

1. The factory produces only one product and sells that product to less than ten customers at a rate of 500 peak megawatts/year.
2. The costs reflect today's technology in terms of the level of automation, throughput, maturity of process, etc.
3. Overhead charges can be defined for a new, dedicated factory and need not be patterned after any existing factory.

In order to perform a detailed cost analysis, a methodology was first developed with general inputs and assumptions being defined. It must be cautioned at this time that Motorola's methodology may differ from methodologies used by the other Task IV contractors performing a similar study. This means, thus, that differences in assumptions and cost inputs by each contractor will

result in different cost allocations per category. The most meaningful comparison between various contractor's cost analyses must be made on the Total Cost basis. Further, costs were developed on an individual process step basis, but meaningful cost analysis for solar cell manufacturing can only be made for a total process sequence. Each process step cost must, then, be placed in a viable process sequence, and adjusted for the total process sequence yield following that step in order to have a true significance in manufacturing cost analysis. In order to allow this adjustment to be made, individual processing step costs are being calculated on a 100% yield basis, with a probable process yield percentage being estimated for use in subsequent process sequence yield calculations.

Results of the costing study of each process step are presented in Table 6-1.

TABLE 6-1

COST SUMMARY

TODAY'S TECHNOLOGY

($/WATT)

PROCESS STEP	MATERIALS	EXPENSE ITEMS	LABOR	OVERHEAD	INTEREST	DEPRECIATION	TOTAL	PROCESS YIELD %	CAPITAL EQUIPMENT	FACILITIES
1. Brushing	0.0	.0073	.0134	.0066	.0023	.0031	.0327	99.5	.0205	.0053
2. Plasma (Dielectric Etch)	0.0	.0031	.0084	.0050	.0064	.0096	.0425	99.8	.0663	.0053
3. Standard Solutions	0.0	.0041	.0061	.0042	.0006	.0005	.0155	99.8	.0031	.0032
4. Centrifuge Drying	0.0	.0014	.0042	.0035	.0003	.0002	.0096	99.8	.0013	.0015
5. Silicon Etching (one side)	0.0	.0124	.0243	.0102	.0012	.0012	.0493	99.5	.0076	.0063
6. Silicon Etching (two sides)	0.0	.0161	.0243	.0102	.0012	.0012	.0530	99.5	.0076	.0063
7. Texture Etch	0.0	.0097	.0243	.0102	.0012	.0011	.0465	99.6	.0068	.0063
8. Edge Grinding	0.0	.0209	.0269	.0113	.0046	.0061	.0698	?	.0407	.0106
9. Photo-Resist (Apply-Expose-Dev.)	0.0	.0107	.0403	.0159	.0073	.0097	.0839	99.4	.0648	.0160
10. Photo-Resist (Remove)	0.0	.0213	.0061	.0042	.0006	.0006	.0328	99.7	.0034	.0032
11. Plasma (P.R. Remove)	0.0	.0009	.0084	.0049	.0004	.0003	.0149	99.9	.0016	.0026
12. Dielectric Etch (Wet)	0.0	.0044	.0081	.0047	.0004	.0004	.0180	99.6	.0023	.0021
13. Etch Stop (Apply)	0.0	.0091	.0067	.0044	.0023	.0031	.0256	99.8	.0211	.0047
14. Spin-On	0.0	.0154	.0067	.0044	.0023	.0031	.0319	--	.0211	.0047

COST SUMMARY
TODAY'S TECHNOLOGY
($/WATT)

PROCESS STEP	MATERIALS	EXPENSE ITEMS	LABOR	OVERHEAD	INTEREST	DEPRECIATION	TOTAL	PROCESS YIELD %	CAPITAL EQUIPMENT	FACILITIES
15. Spray-On	0.0	.0152	.0034	.0032	.0011	.0014	.0243	--	.0095	.0023
16. Drive-In (Diffusion)	0.0	.0099	.0102	.0057	.0026	.0032	.0316	99.5	.0212	.0081
17. Silicon Source (Solid)	0.0	.0173	.0407	.0161	.0053	.0065	.0859	98.0	.0423	.0162
18. Gas Depositon and Diffusion	0.0	.0174	.0102	.0057	.0026	.0032	.0391	99.0	.0212	.0081
19. Doped Oxide (CVD)	0.0	.0174	.0102	.0057	.0026	.0032	.0391	99.0	.0212	.0081
20. Ion Implant	0.0	.0097	.0746	.0357	.1406	.2029	.4635	98.0	1.390	.1723
21. Ion Implant (Advanced)	0.0	.0014	.0022	.0030	.0067	.0101	.0234	99.5	.0695	.0052
22. Vacuum Metallization Cu, Al	.0024	.0490	.0318	.0146	.0236	.0326	.1540	99.0	.2211	.0413
23. Thick Film Ag Front	.0457	.0040	.0060	.0040	.0011	.0016	.0624	99.8	.0107	.0018
24. Thick Film Ag Back	.1988	.0040	.0060	.0040	.0011	.0016	.2155	99.8	.0107	.0018
25. Electroless Plating	.0305	.0256	.0145	.0089	.0011	.0012	.0818	99.6	.0073	.0049
26. Electrolytic Plating	.0305	.0256	.0145	.0089	.0011	.0012	.0818	99.6	.0073	.0049
27. Solder Coating	.0223	.0002	.0014	.0025	.0002	.0003	.0269	99.8	.0021	.0005
28. Silicon Nitride (CVD)	0.0	.0098	.0102	.0057	.0026	.0032	.0315	99.8	.0212	.0081
29. Oxide Growth	0.0	.0049	.0051	.0039	.0013	.0016	.0168	99.8	.0106	.0040

COST SUMMARY
TODAY'S TECHNOLOGY
($/WATT)

PROCESS STEP	MATERIALS	EXPENSE ITEMS	LABOR	OVERHEAD	INTEREST	DEPRECIATION	TOTAL	PROCESS YIELD %	CAPITAL EQUIPMENT	FACILITIES
30. Spin-On	0.0	.0079	.0067	.0044	.0023	.0031	.0244	97.0	.0211	.0047
31. Evaporate	.0019	.0022	.0318	.0146	.0236	.0326	.1067	99.0	.2211	.0413
32. Add Solder	.0014	.0001	.0007	.0022	.0001	.0001	.0046	99.8	.0008	.0002
33. Reflow Solder	0.0	.0001	.0170	.0032	.0008	.0011	.0222	99.8	.0074	.0015
34. Conductive Adhesives	.0045	.0002	.0060	.0040	.0011	.0016	.0174	99.5	.0107	.0018
35. Glass Superstrate	.1817	.0004	.0006	.0027	.0012	.0010	.1876	99.4	.0057	.0074
36. Glass with Substrate	.3448	.0004	.0006	.0027	.0013	.0011	.3509	99.0	.0063	.0081
37. Electrical Test (cells)	0.0	.0001	.0085	.0048	.0008	.0012	.0154	99.8	.0079	.0011
38. Electrical Test (modules)	0.0	.0000	.0003	.0021	.0001	.0001	.0026	99.8	.0010	.0002

A more detailed cost analysis with refined assumptions was performed during the second year of this contract and is reported in Section 4.